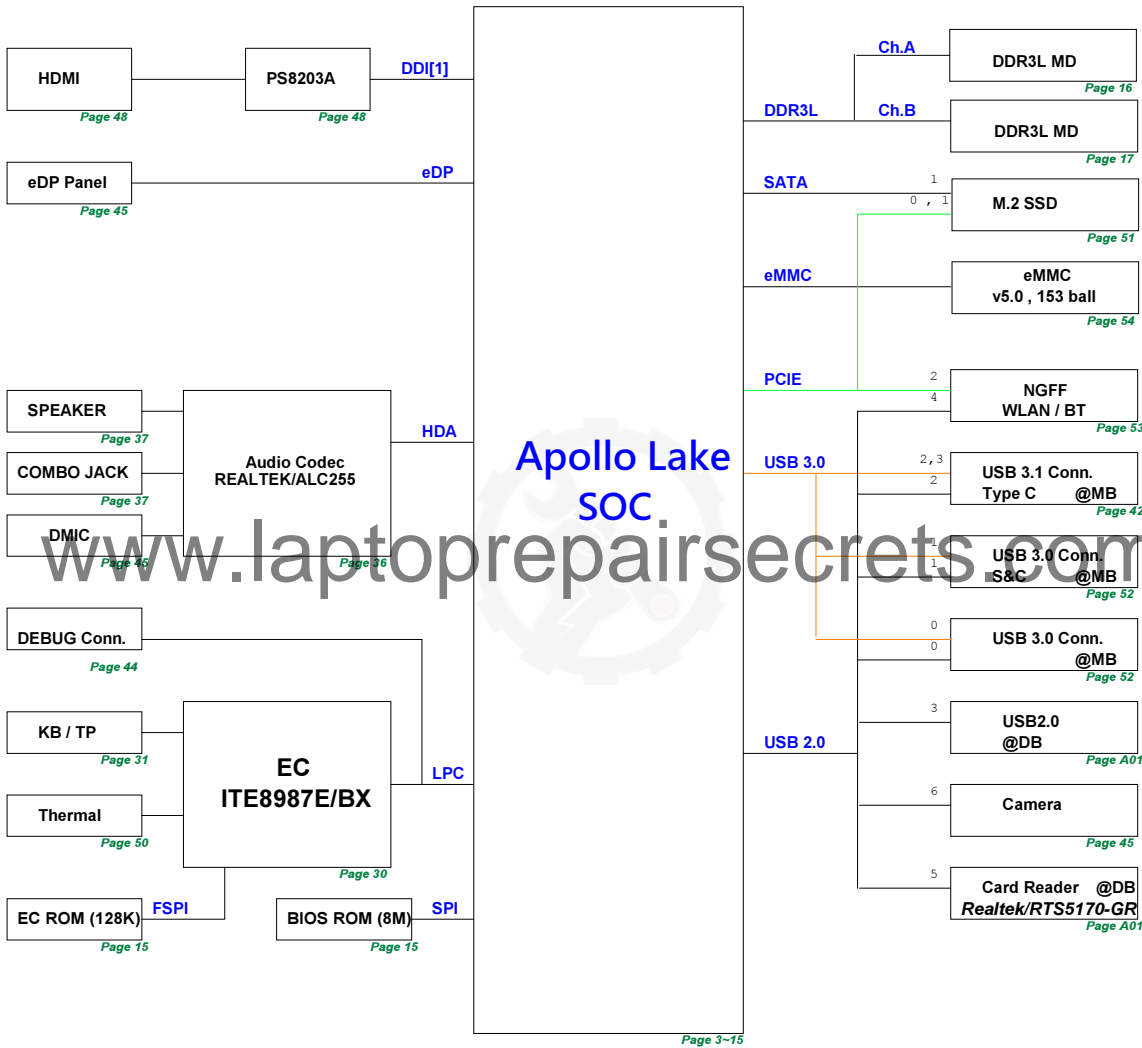


Armani with Intel Apollo Lake Block Diagram



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Discharge Circuit
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DC & BATT. Conn.
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Skew Holes
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Power

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System (5V & 3V)
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+1.05VS
Page 82

DDR & VTT
Page 83

+1.8VSUS
Page 84

+1.24 VSUS
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BATTERY CHARGER
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Powewr DETECT
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LOAD SWITCH
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Power Protect
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 - 04. CPU(3)_USB,PCIE,SATA,SMBus
 - 05. CPU(4)_DDI,MIPI,EMMC,SDIO
 - 06. CPU(5)_I2C,LPC
 - 07. CPU(6)_RTC
 - 08. CPU(7)_GPIO
 - 09. CPU(8)_POWER
 - 10. CPU(9)_GND
 - 12. CPU(10)_LEVEL_SHIFT
 - 13. CPU(11)_APL HW STRAPS
 - 15. CPU(13)_SPI,SMB
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 - 17. DDR3L_MEMORY DIMM
 - 18. DDR voltage
 - 30. EC ITE8987E/BX
 - 31. TP / Keyboard
 - 32. RST_Reset Circuit
 - 36. Audio Codec
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 - 41. USB 3.1 Type-C
 - 44. BUG_Debug
 - 45. eDP_output
 - 48. HDMI
 - 50. THERMAL
 - 51. M.2 SSD
 - 52. USB3.0_Charge IC
 - 53. NGFF_WLAN/BT
 - 55. PCIe re-Driver
 - 57. Discharge
 - 60. DC-IN/ Batt connector
 - 62. TPM_NPT65x
 - 65. ME_CONN,Skew Hole
 - 66. IO Board CONN
 - 69. Finger printer
 - 80. POWER_VCORE
 - 81. POWER_SYSTEM
 - 82. POWER_1.05VS
 - 83. POWER_DDR & VTT
 - 84. POWER_1.8VSUS
 - 85. POWER_1.24VSUS
 - 88. POWER_CHARGER
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 - 91. POWER_LOAD SWITCH
 - 92. POWER_PROTECT
 - 93. POWER_SIGNAL
 - 94. POWER_FLOWCHART
 - 97. POWER_TREE
 - 98. POWER_HISTORY
 - 99. POWER_SEQUENCE
 - A01. IO Board , CR , USB2 , LED

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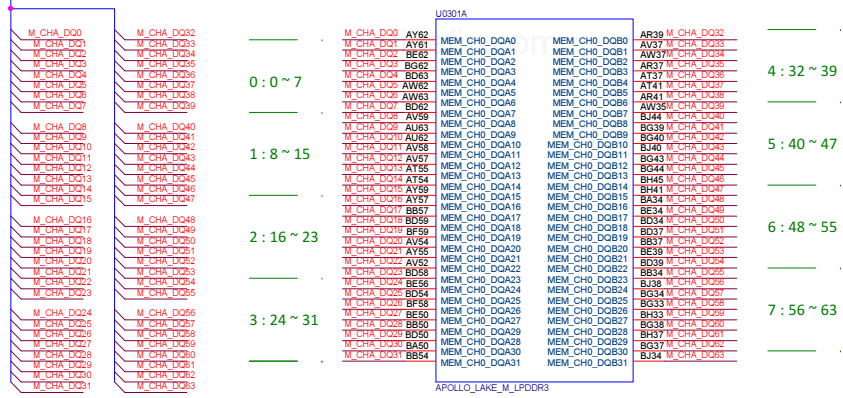
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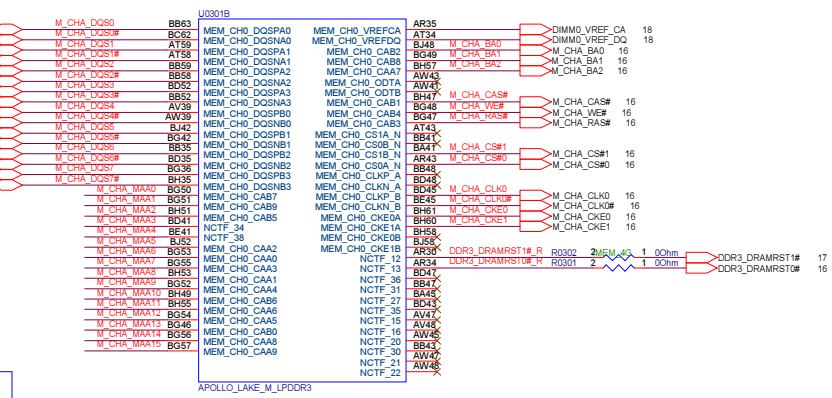
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PEGATRON PROPRIETARY AND CONFIDENTIAL		Engineer: Raly Hsieh	
Size A	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet 2 of 100	

DRAM Channel 0

16 M_CHA_DQ[0..63]



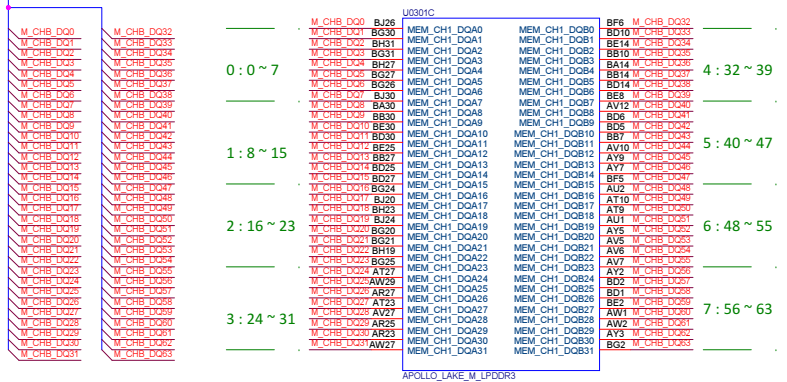
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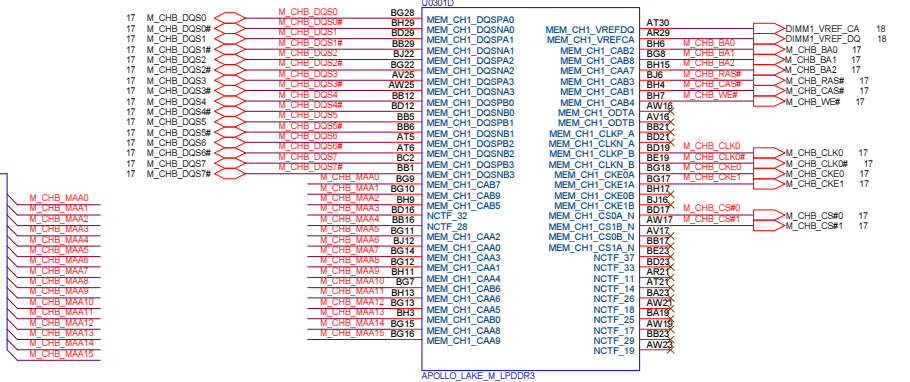
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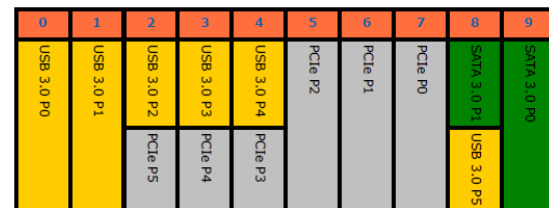
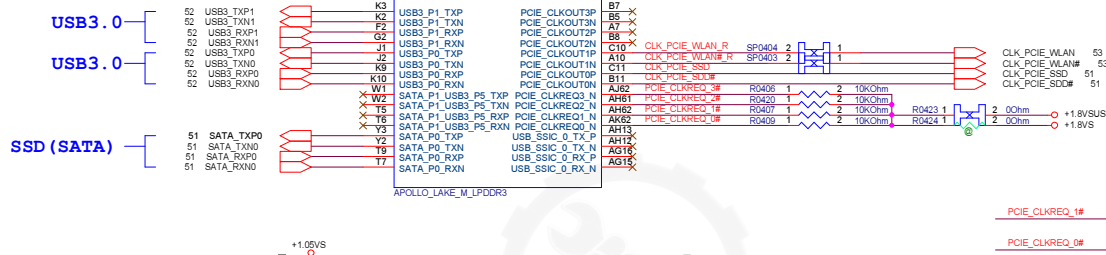
DRAM Channel 1

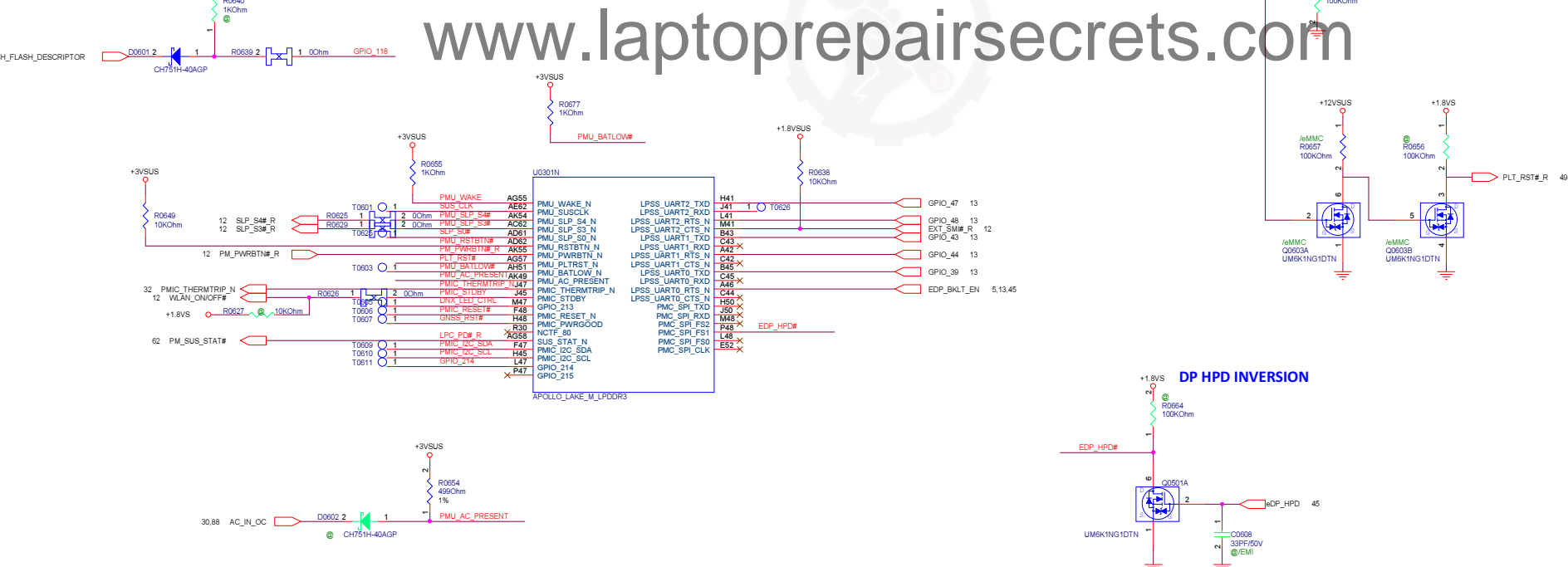
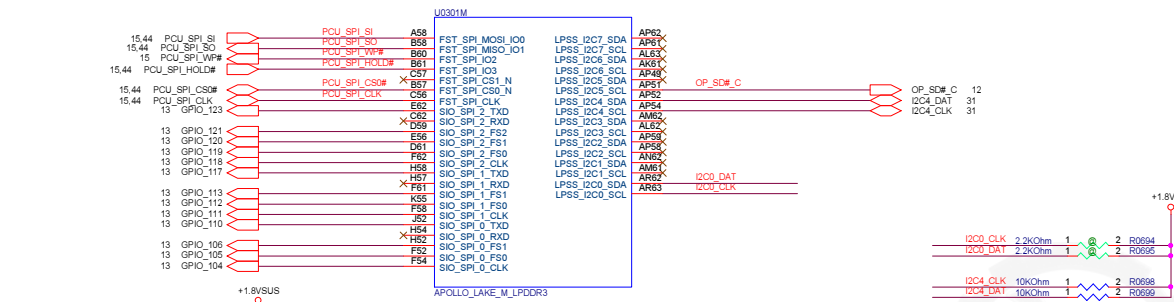
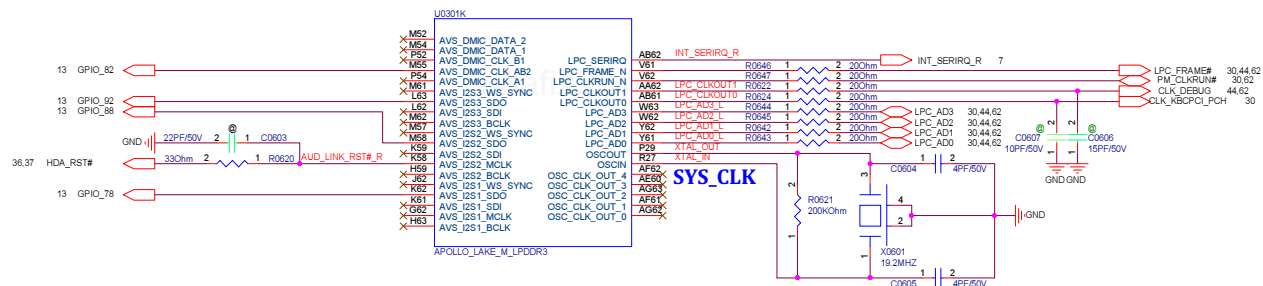
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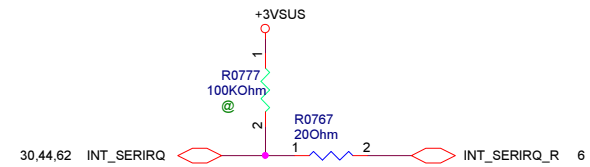
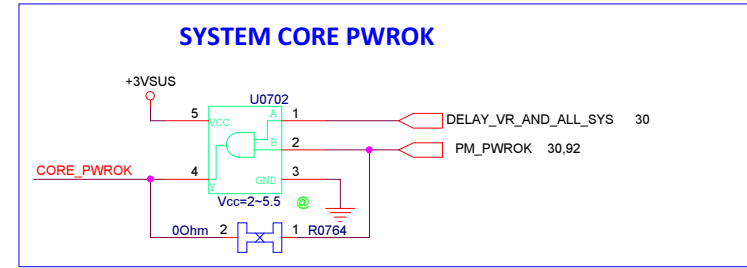
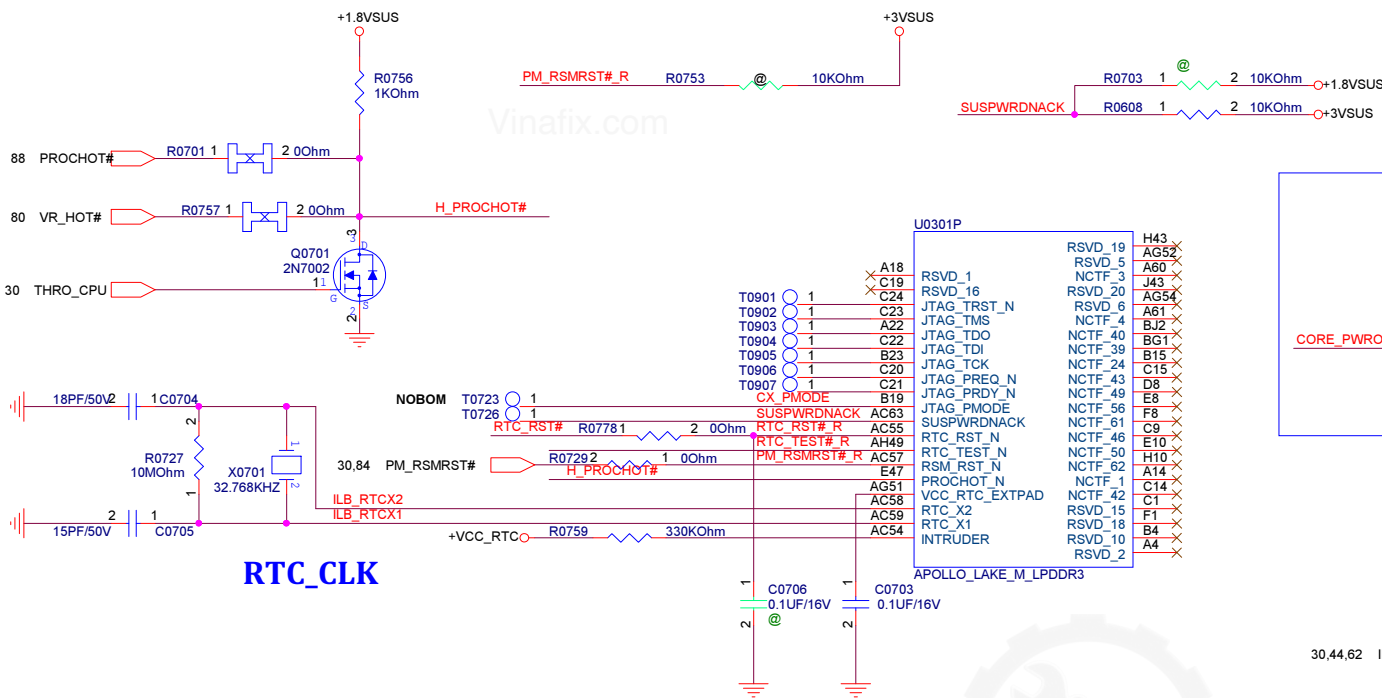
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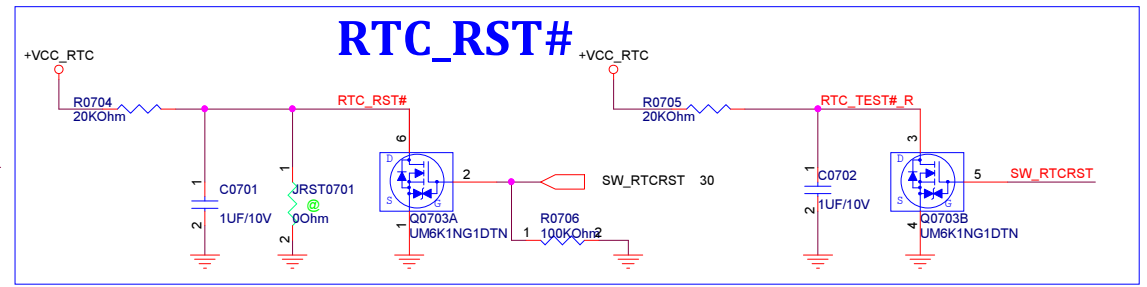
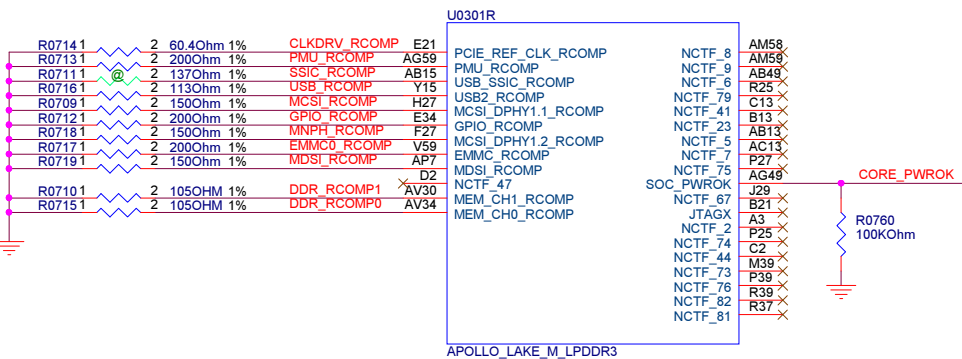




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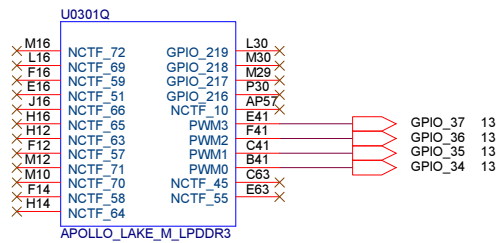
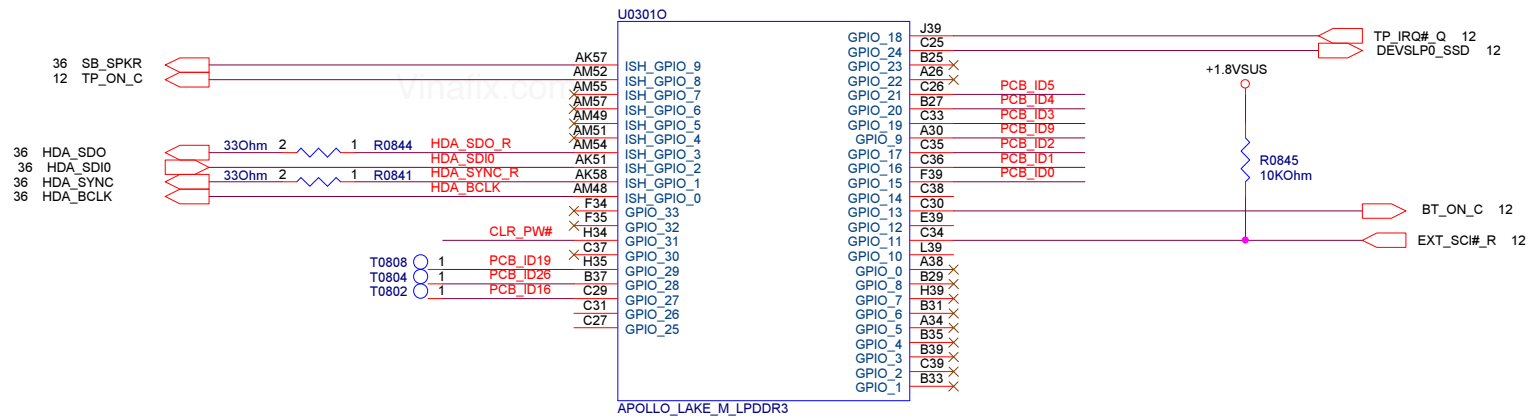


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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: Raly Hsieh	
Size	Project Name	Rev	
B	AS3EA	2.0	
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www.laptoprepairsecrets.com BIOS Rev. SKU

ID2	ID1	ID0	PCB Rev.
0	0	0	R1.0
0	0	1	R1.1
0	1	0	R2.0
0	1	1	TBD
1	0	0	TBD
1	0	1	TBD
1	1	0	TBD
1	1	1	TBD

PCB_ID9

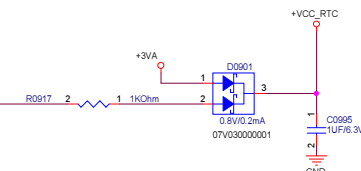
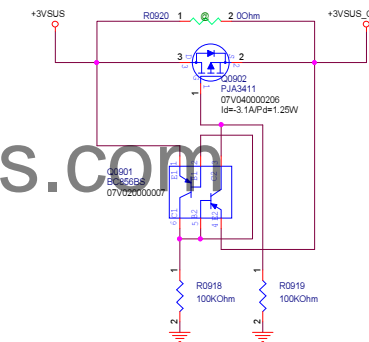
1: eMMC
0: Non-eMMC

PCB_ID4

1: SATA SSD
0: PCIE SSD

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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: Raly Hsieh	
Size	Project Name		Rev
B	AS3EA		2.0
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: Raly Hsieh	
Size	Project Name		Rev
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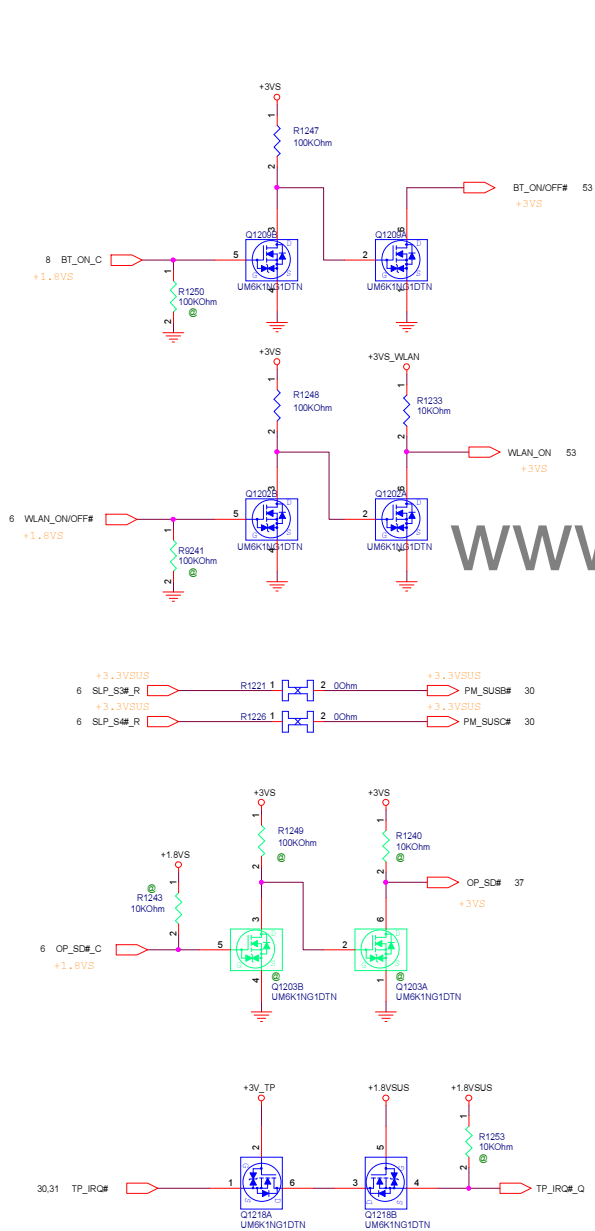
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Size C	Project Name AS3EA	Rev 2.0	
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Apollo Lake to Device

+3V		+3V	31,44,45,57,91
+3VS		+3VS	6,30,31,32,36,37,41,45,48,49,50,51,53,57,62,66,91,92
+3VS_WLAN		+3VS_WLAN	53
+3VSUS		+3VSUS	4,6,7,9,10,30,31,45,53,57,62,80,81,84,85,92
+VS		+VS	31,36,48,57,69,91
+12VSUS		+12VSUS	6,81,91

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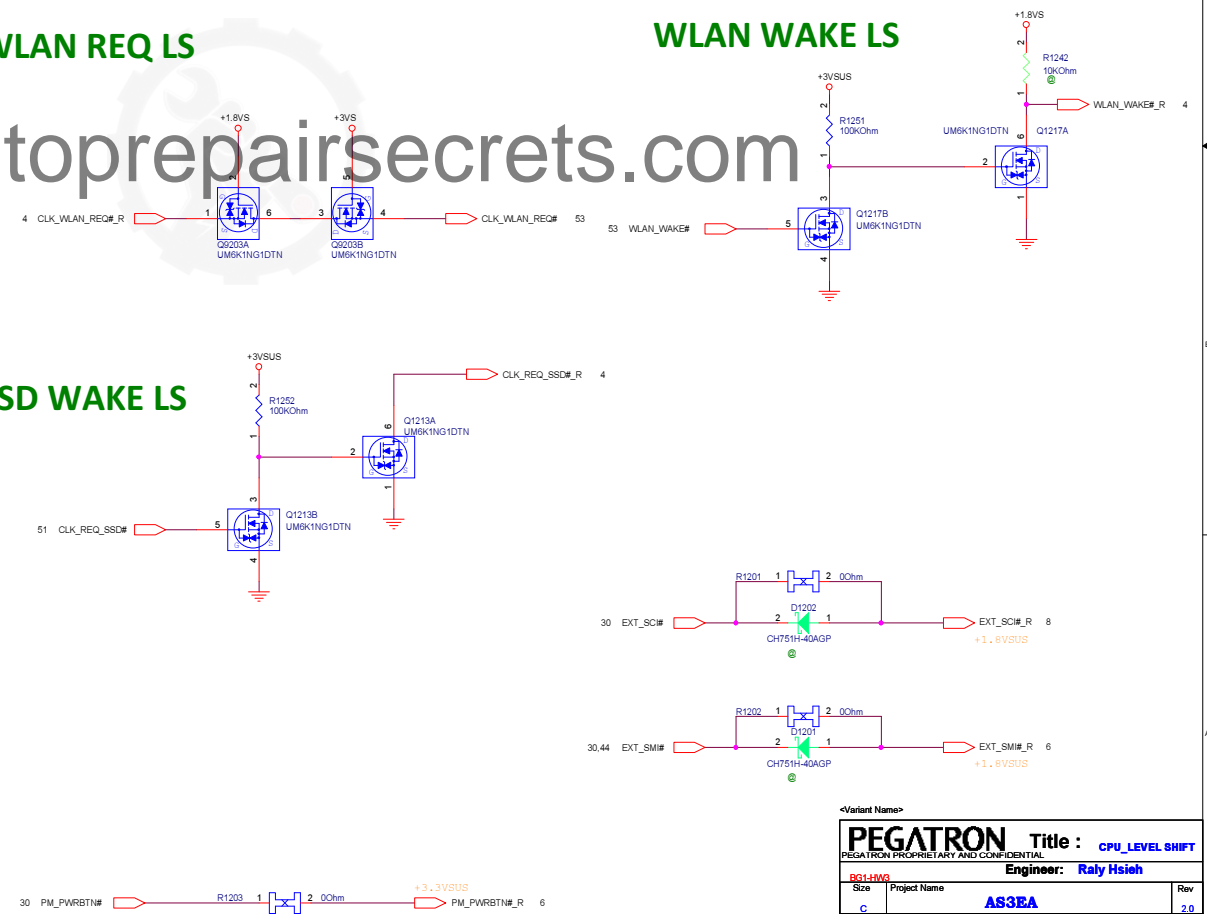


Device to Apollo Lake

WLAN REQ LS

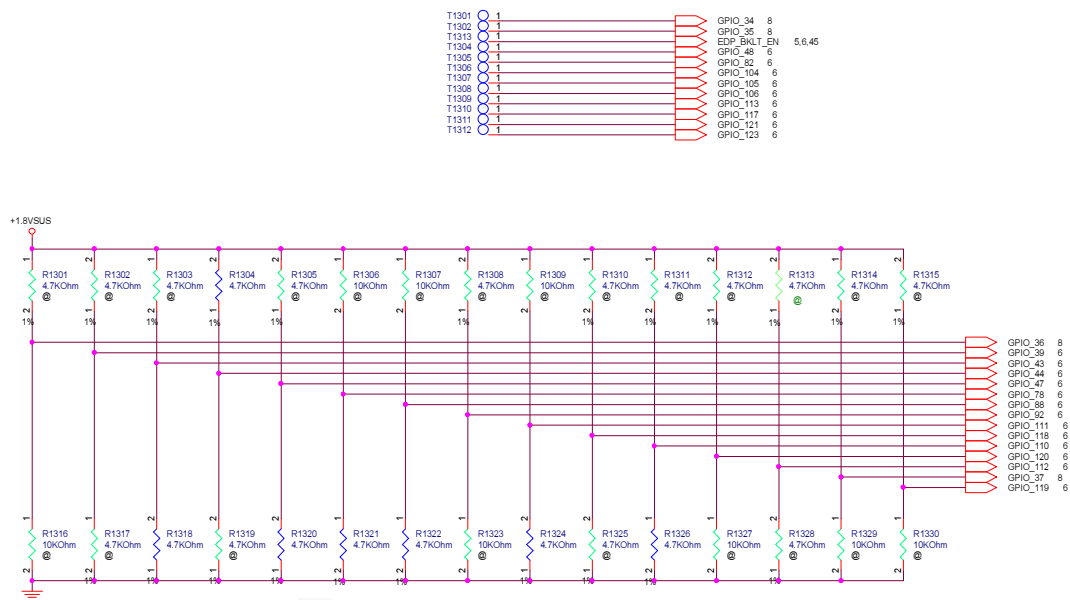
WLAN WAKE LS

SSD WAKE LS



GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_34	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.
GPIO_35	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.
GPIO_36	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.
GPIO_39	Enable CSE ROM Bypass	20K PD	<p>1 = enable bypass 0 = disable bypass (default)</p> <p>Note:</p> <ol style="list-style-type: none"> SoC supports TXE3.0 (this is also called CSE) This strap tells CSE (TXE3.0) to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of CSE (TXE3.0) before the first patch point this strap enabled the platform tell CSE (TXE3.0) to bypass the ROM causing the issue and go to the patch space instead.
GPIO_40	RTC Clock Timer Bypass	20K PD	<p>1 =enable bypass 0 =disable bypass (default)</p> <p>Note: This strap shall only be used when an external oscillator is used to supply a 32.768kHz clock to RTC_X1.</p>
GPIO_43	RSVD	20K PU	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_44	Allow SPI as a boot source	20K PU	<p>1=enable (default) 0=disable</p>
GPIO_47	Force DNX FW Load	20K PD	<p>1 = Force 0 = Do not force (default)</p> <p>Notes:</p> <ol style="list-style-type: none"> DNX: Download and Execute. This strap is a recovery strap for corrupted FW image. This strap will force CSE (TXE3.0) to execute a "Download and Execute" (DNX) flow, where it would fetch firmware from a USB stick and re-flash a eMMC device. CSE (TXE3.0) can do it for BIOS part of FW, but if CSE FW itself is corrupted we need this strap.
GPIO_48	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	<p>1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode</p>
GPIO_82	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_88	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PU	<p>1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode</p>
GPIO_92	SMBus No Re-Boot	20K PD	<p>1 = Enable 0 = Disable (default)</p> <p>Note: Platforms should strap this LOW. Functionality is handled by the PMC.</p>
GPIO_104	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_105	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_106	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	<p>1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode</p>
GPIO_111	RSVD	20K PU	<ul style="list-style-type: none"> Pull LOW when RSM_RST_N de-asserts to map these regions to the boot SPI Pull HIGH when RSM_RST_N de-asserts to leave these regions unmapped by the System Agent <p>Note: Pull LOW for designs that boot from SPI and HIGH otherwise</p>
GPIO_112	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_113	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_117	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_118	Flash Descriptor Override	20K PD	<p>0 = No Override (Normal Operation) 1 = Override</p> <p>Note: This strap enables the platform to override security features in the SPI.</p>
GPIO_120	Top swap override	20K PD	<p>1 = Enable 0 = Disable (default)</p> <p>Note: Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.</p>
GPIO_121	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_123	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.



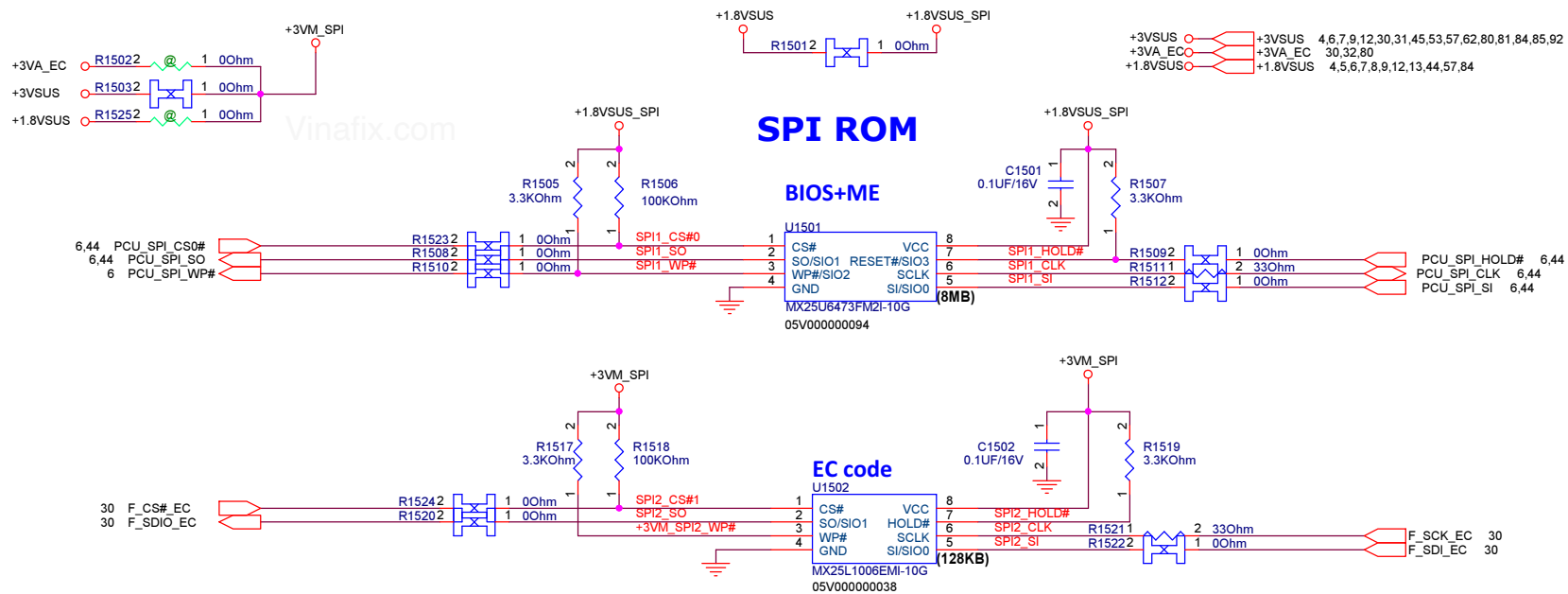
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BG1-HW0		Engineer: Raly Hsieh	
Size	Project Name	Rev	
C	AS3EA	2.0	
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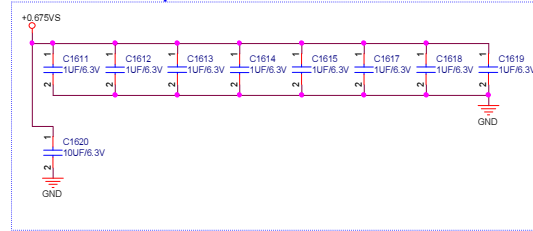
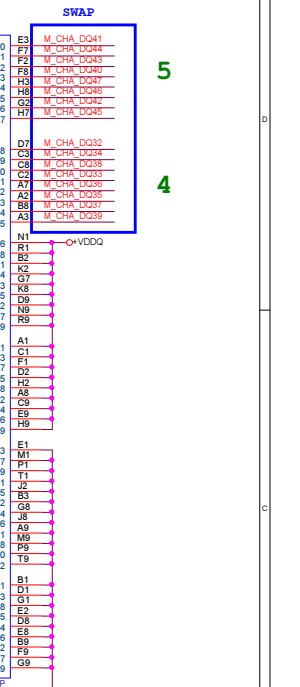
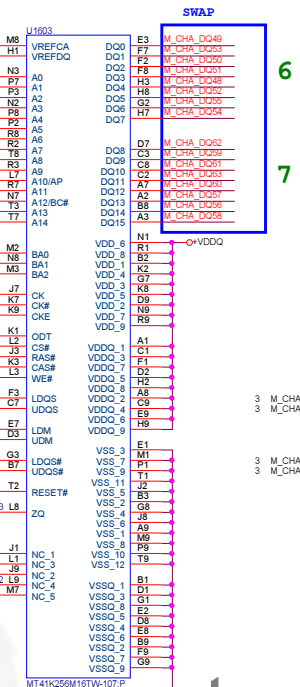
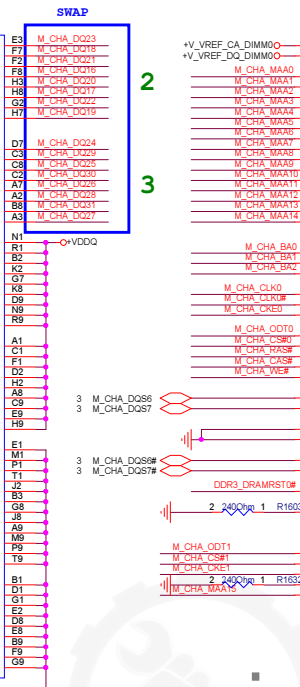
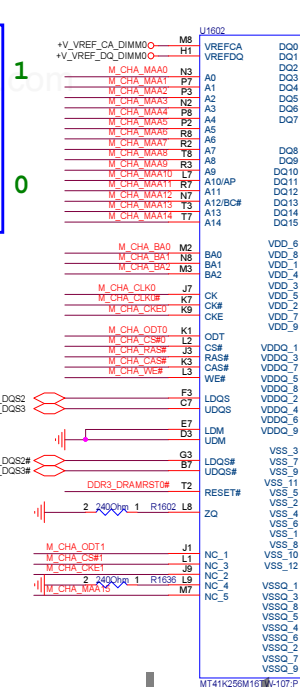
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PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 Engineer: Raly Hsieh

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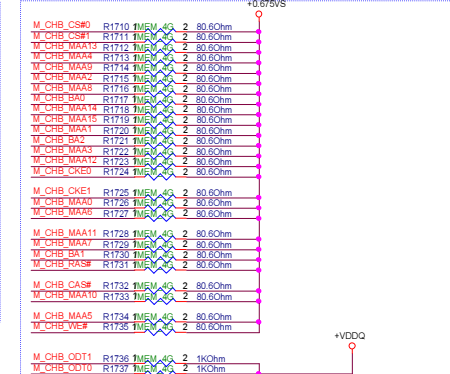
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Terminal Resistor



A circuit diagram showing a resistor R1738 with a value of 80.80 Ohms. The resistor is connected between two nodes: M_CHB_CLK0 and MEM_4G. The node M_CHB_CLK0 is labeled with a red 'X' and the node MEM_4G is labeled with a green 'X'.

+V_VREF_DQ_DIMM0		+V_VREF_DQ_DIMM0	16
+V_VREF_CA_DIMM0		+V_VREF_CA_DIMM0	16
+V_VREF_CA_DIMM1		+V_VREF_CA_DIMM1	17
+V_VREF_DQ_DIMM1		+V_VREF_DQ_DIMM1	17
+VDDQ		+VDDQ	9,16,17,57,83



M3



PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL		<u>LPDDR3(3)_CA/DO Voltage</u>	
Engineer: Raly Hsieh			
BG1-FW3			
Size	Project Name		Rev
Custom	AS3EA		2.0
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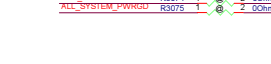
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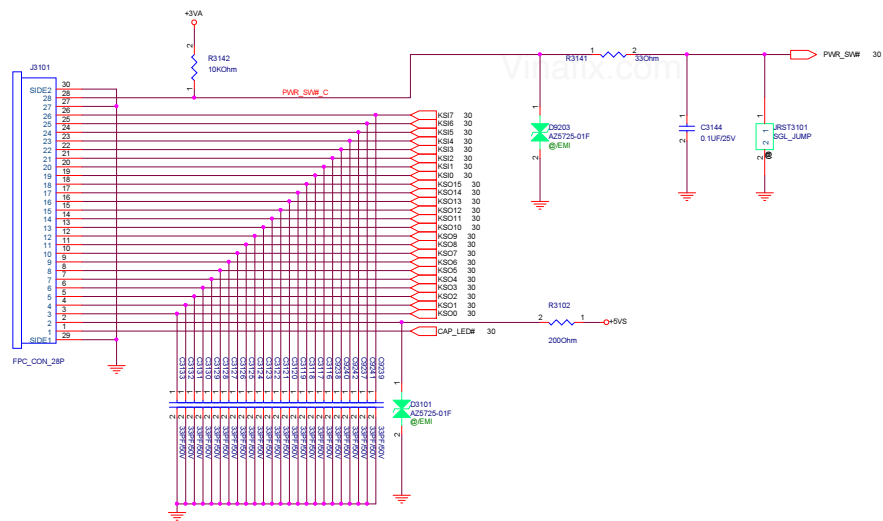
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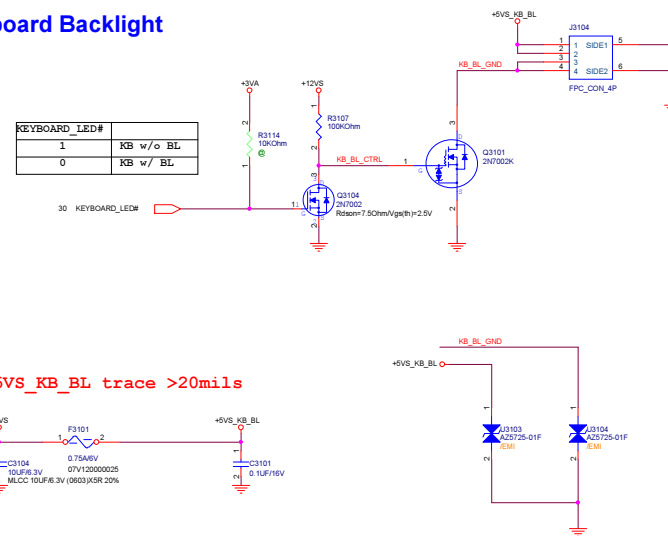
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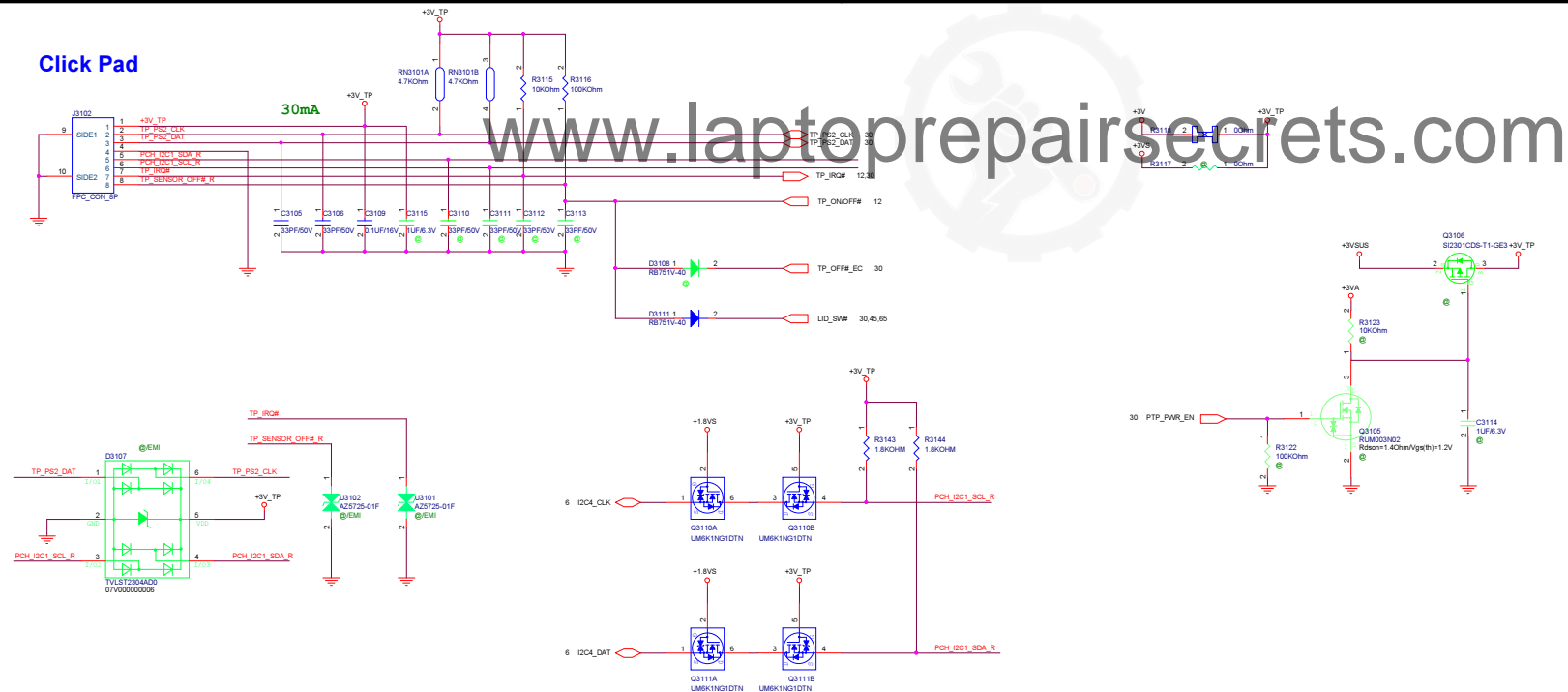
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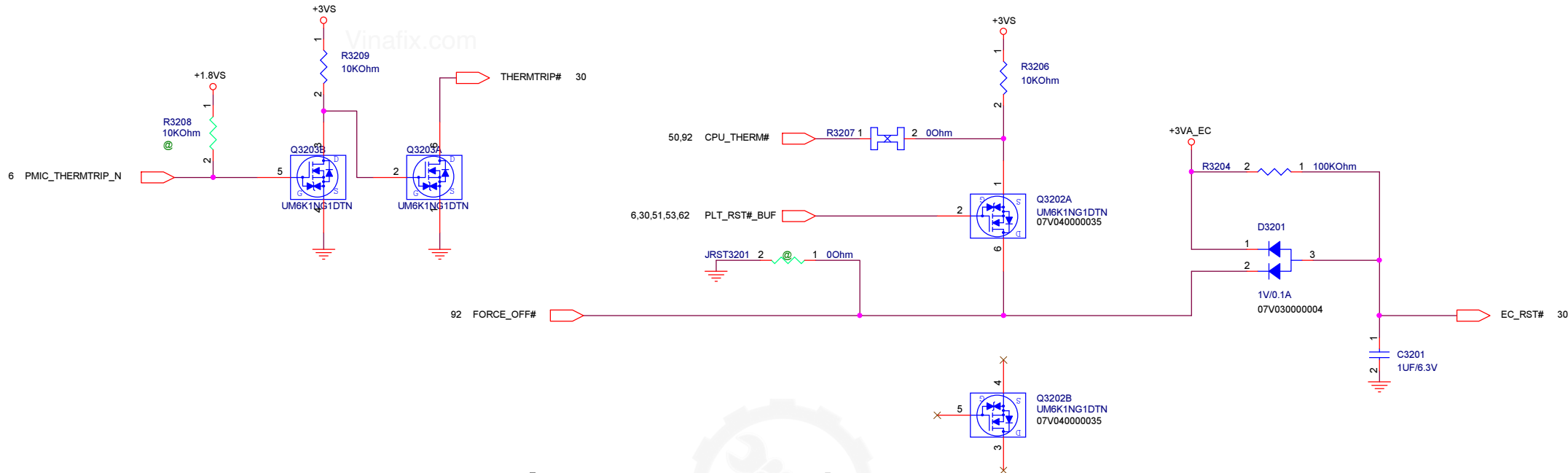


Keyboard Backlight



Click Pad





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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: Raly Hsieh	
Size	Project Name		Rev
Custom	AS3EA		2.0
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<Variant Name>

PEGATRON		Title Realtek RTL8111G	
PEGATRON PROPRIETARY AND CONFIDENTIAL		Raly Hsieh	
Engineer:			
Size Custom	Project Name AS3EA	Rev 33	Rev 100
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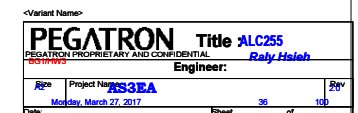
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PEGATRON		Title : RJ45	
BG1/HW3		Engineer: Raly Hsieh	
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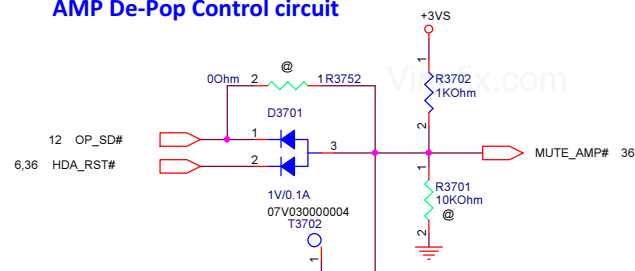
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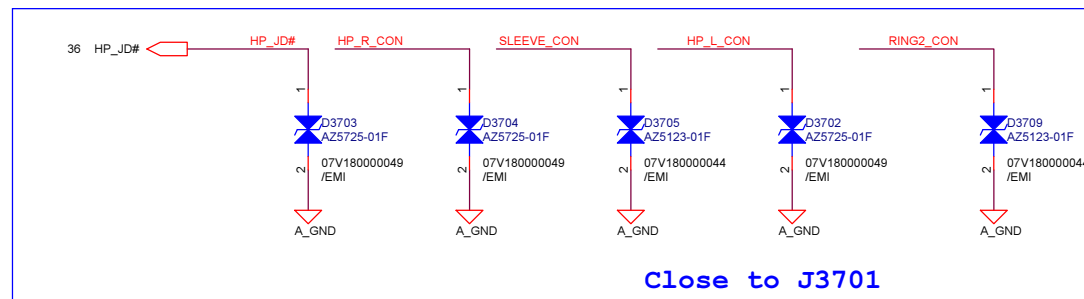
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Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	35 of 100



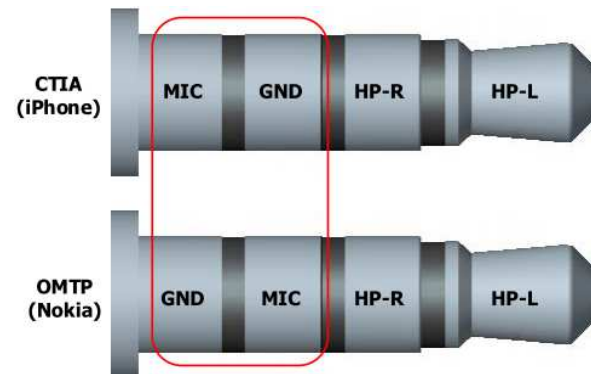
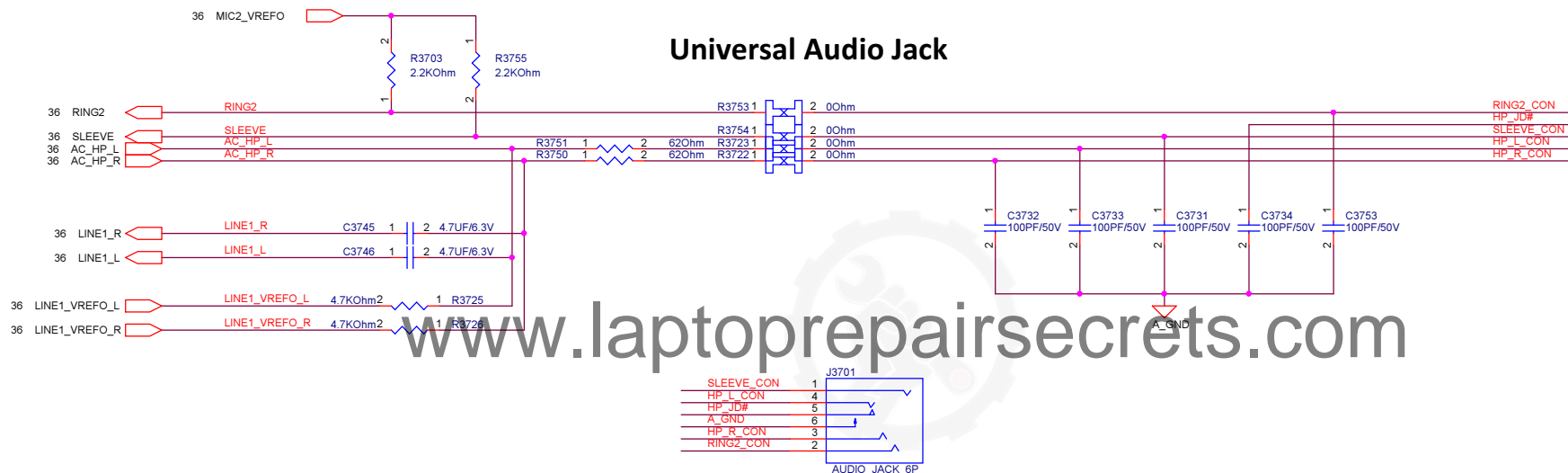
AMP De-Pop Control circuit



+3VS +3VS 6,12,30,31,32,36,41,45,48,49,50,51,53,57,62,66,91,92



Universal Audio Jack



<Variant Name>

PEGATRON Title :COMBO JACK
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Raly Hsieh

Size Project Name AS3EA Rev 2.0

Date: Monday, March 27, 2017 Sheet 37 of 100

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www.laptoprepairsecrets.com

<Variant Name>			
PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	38 of 100

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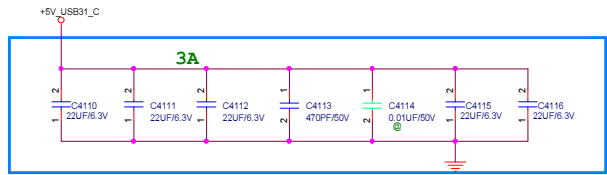
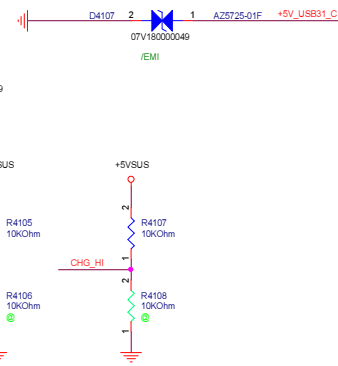
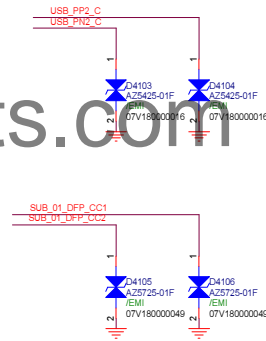
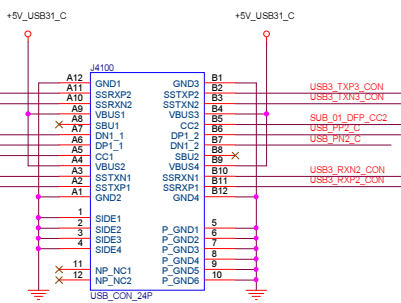
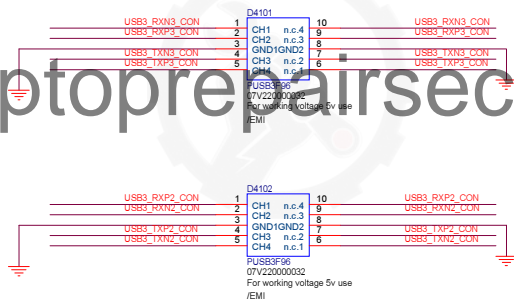
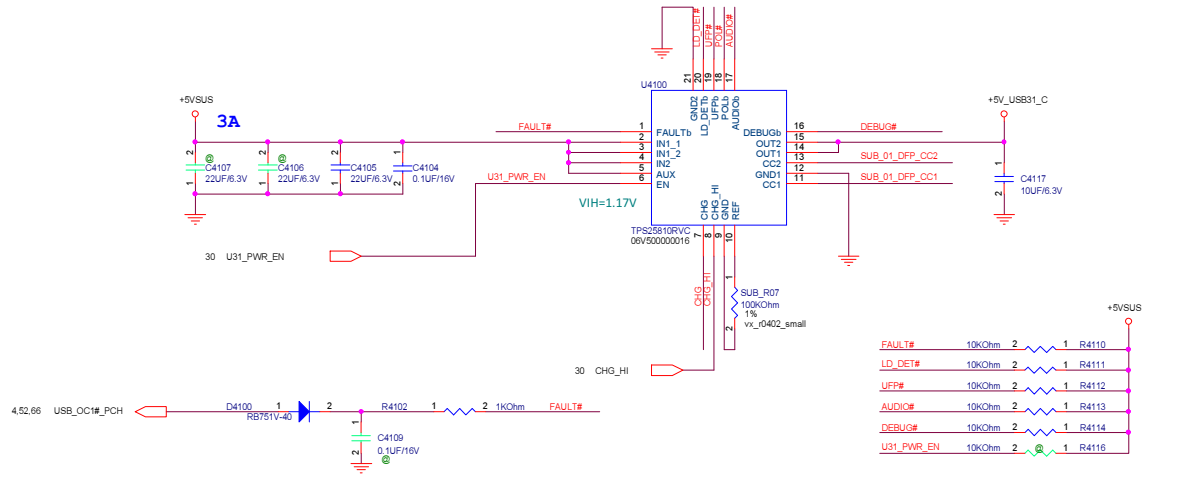
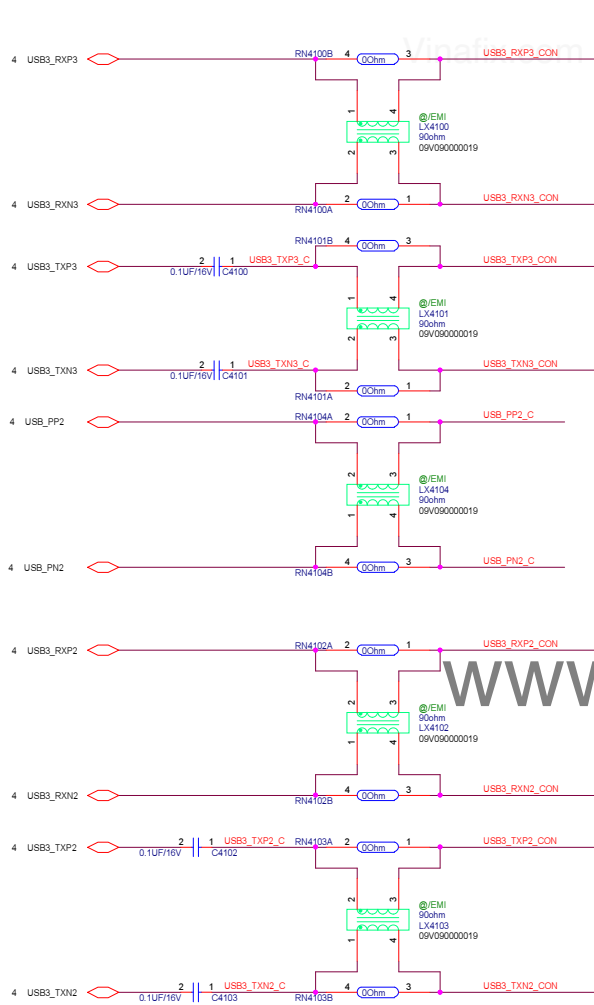
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	39 of 100

Vinafix.com

www.laptoprepairsecrets.com

PEGATRON		Title : 40. card reader	
BG1/HW3		Engineer: Raly Hsieh	
Size	Project Name		Rev
Custom	AS3EA		2.0
Date: Monday, March 27, 2017		Sheet	40 of 100

USB3.1 Type C TPS25810



near connector

Vinafix.com

www.laptoprepairsecrets.com

<Variant Name>

PEGATRON		Title USB Type-C Receptacle	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Raly Hsieh	
Size Custom	Project Name AS3EA		Rev 2.0
Date: Monday, March 27, 2017	Sheet 42 of 100		

Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than 5V to operate correctly, execute the steps below in the order they are listed:

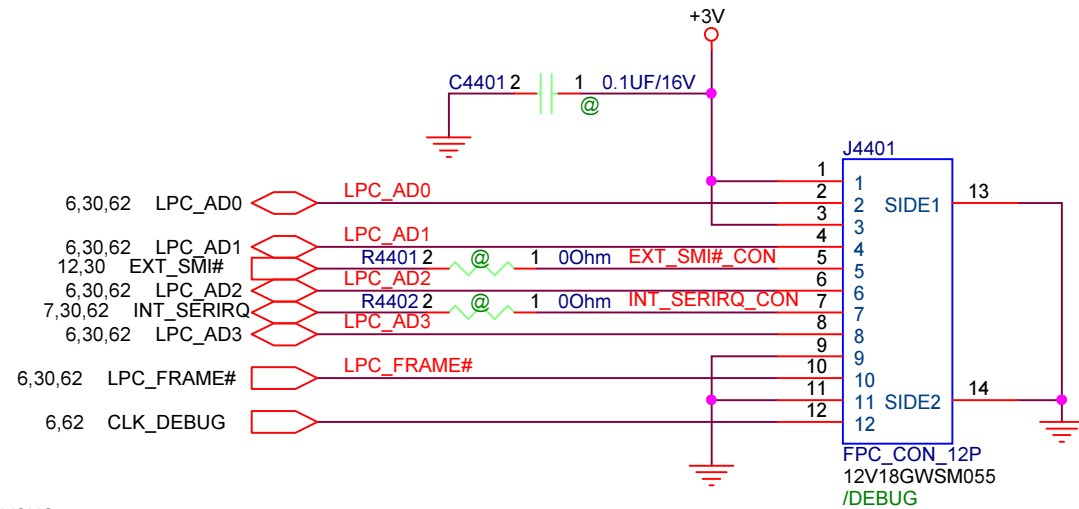
Vinafix.com

www.laptoprepairsecrets.com

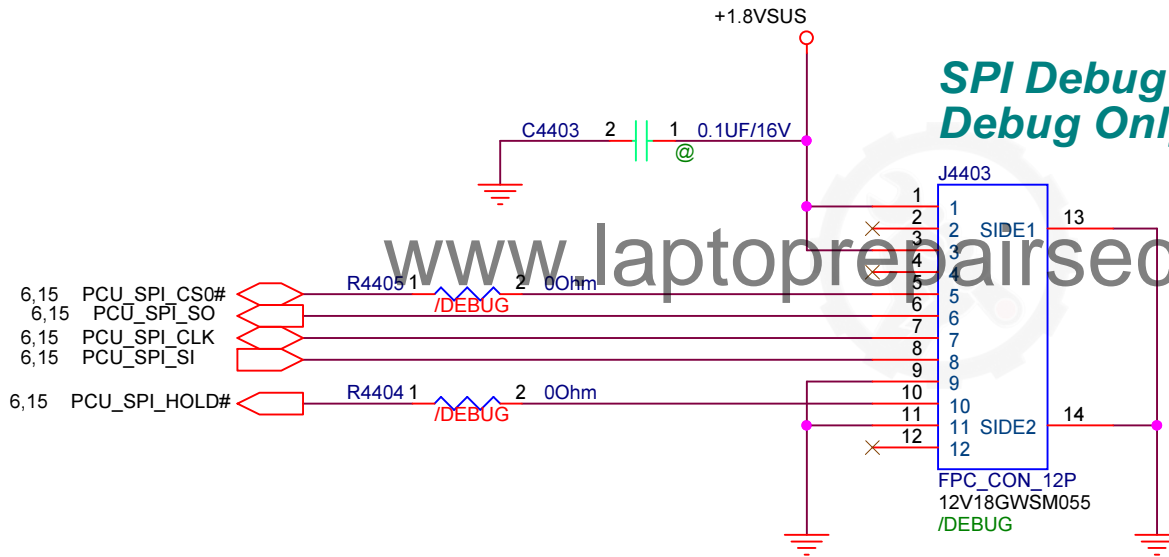
<Variant Name>

PEGATRON		Title : Dead Battery	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Raly Hsieh	
Size Custom	Project Name AS3EA		Rev 2.0
Date: Monday, March 27, 2017		Sheet 43 of 100	

Vinafix.com



SPI Debug Port Debug Only



<Variant Name>

PEGATRON Title : **BUG_Debug**
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: **Raly Hsieh**

BG1-HW3

Size

Project Name

Rev

Custom

AS3EA

2.0

Date: **Monday, March 27, 2017**

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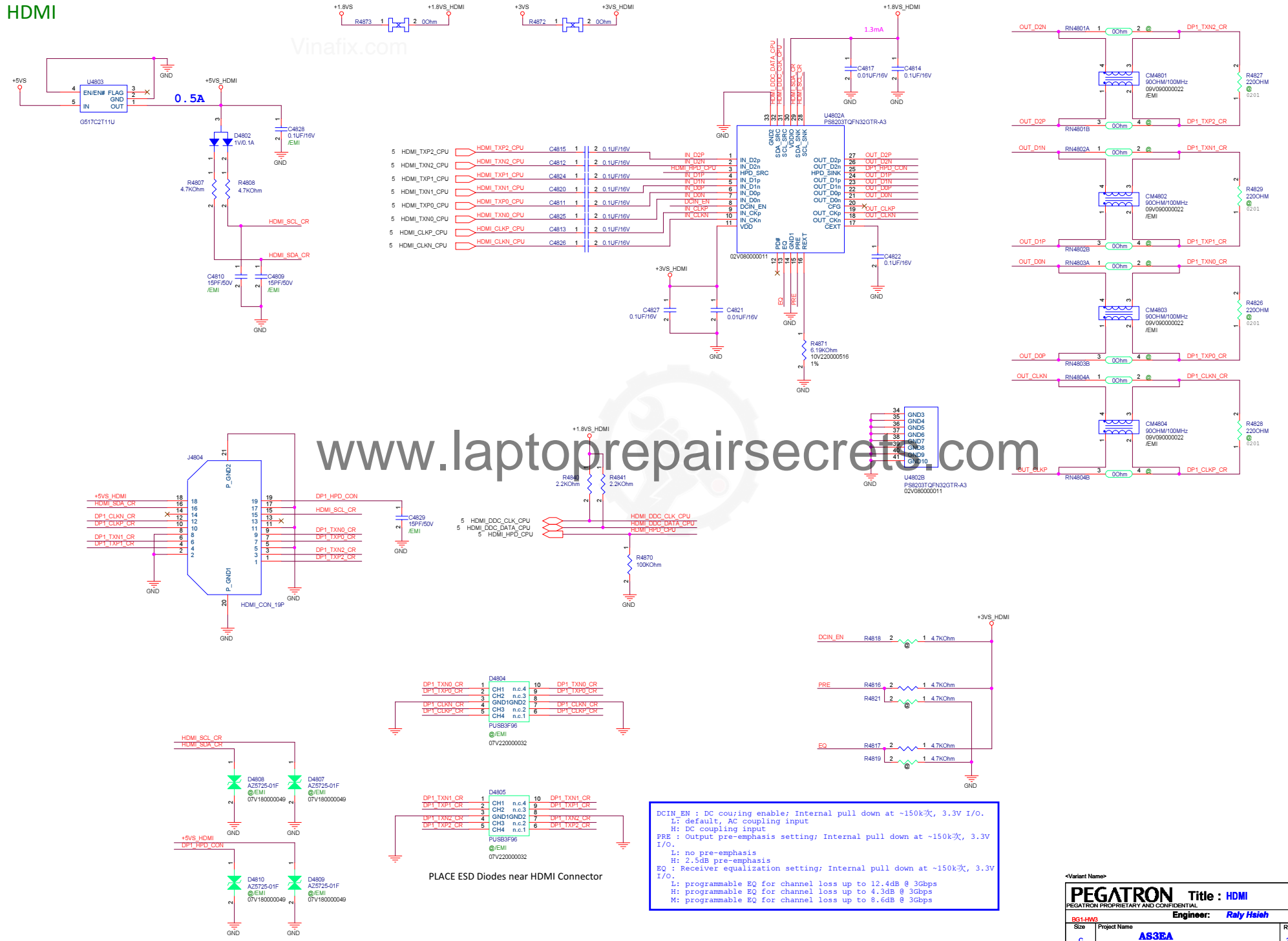
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	46 of 100

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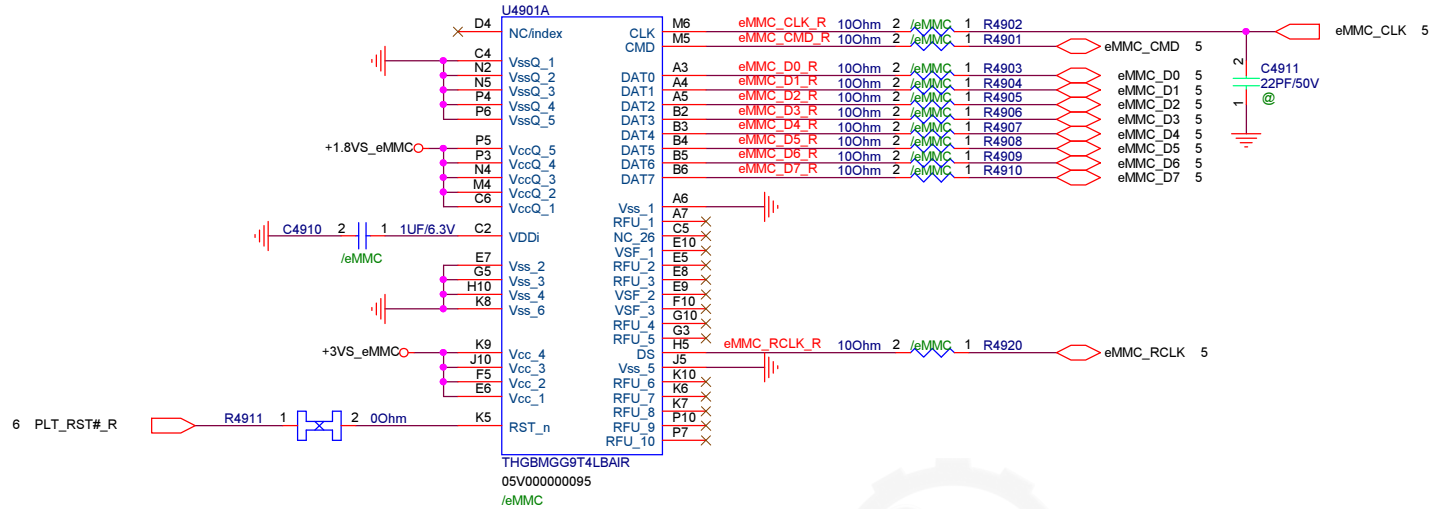
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
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Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	47 of 100

HDMI

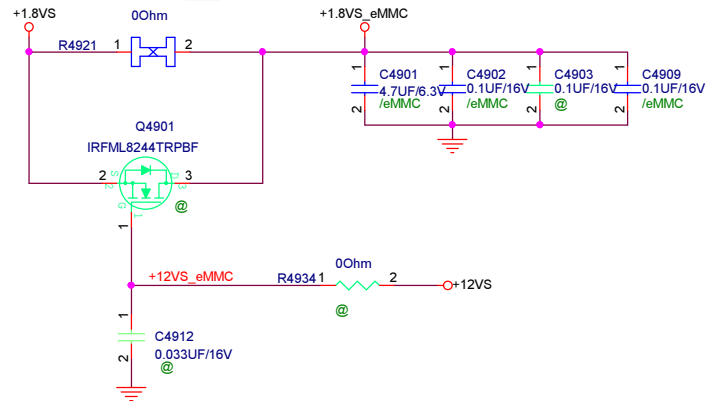
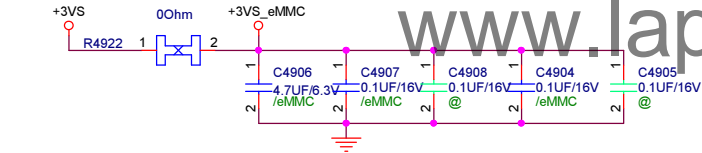


49 EMMC

Vinafix.com



A1	NC_1	H12
A10	NC_2	H13
A11	NC_3	H14
A12	NC_4	H2
A13	NC_5	H3
A14	NC_6	J1
A2	NC_7	J2
A8	NC_8	J3
A9	NC_9	J4
B1	NC_10	J5
B10	NC_11	J6
B11	NC_12	J7
B12	NC_13	J8
B13	NC_14	J9
B14	NC_15	J10
B7	NC_16	J11
B8	NC_17	J12
B9	NC_18	J13
C1	NC_19	J14
C10	NC_20	J15
C11	NC_21	J16
C12	NC_22	J17
C13	NC_23	J18
C14	NC_24	J19
C3	NC_25	J20
C7	NC_26	J21
C8	NC_27	J22
C9	NC_28	J23
D1	NC_29	J24
D12	NC_30	J25
D13	NC_31	J26
D14	NC_32	J27
D2	NC_33	J28
D3	NC_34	J29
D4	NC_35	J30
E1	NC_36	J31
E12	NC_37	J32
E13	NC_38	J33
E14	NC_39	J34
E2	NC_40	J35
E3	NC_41	J36
F1	NC_42	J37
F12	NC_43	J38
F13	NC_44	J39
F14	NC_45	J40
F2	NC_46	J41
F3	NC_47	J42
G1	NC_48	J43
G12	NC_49	J44
G13	NC_50	J45
G14	NC_51	J46
G2	NC_52	J47
H1	NC_53	J48



eMMC_D0	R4923	1	2	49.9KOhm	/eMMC
eMMC_D1	R4924	1	2	49.9KOhm	/eMMC
eMMC_D2	R4925	1	2	49.9KOhm	/eMMC
eMMC_D3	R4926	1	2	49.9KOhm	/eMMC
eMMC_D4	R4927	1	2	49.9KOhm	/eMMC
eMMC_D5	R4928	1	2	49.9KOhm	/eMMC
eMMC_D6	R4929	1	2	49.9KOhm	/eMMC
eMMC_D7	R4930	1	2	49.9KOhm	/eMMC
eMMC_CMD	R4931	1	2	10KOhm	/eMMC
PLT_RST#_R	R4932	1	2	49.9KOhm	/eMMC

<Variant Name>

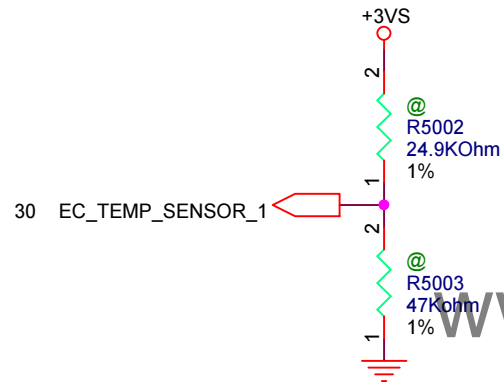
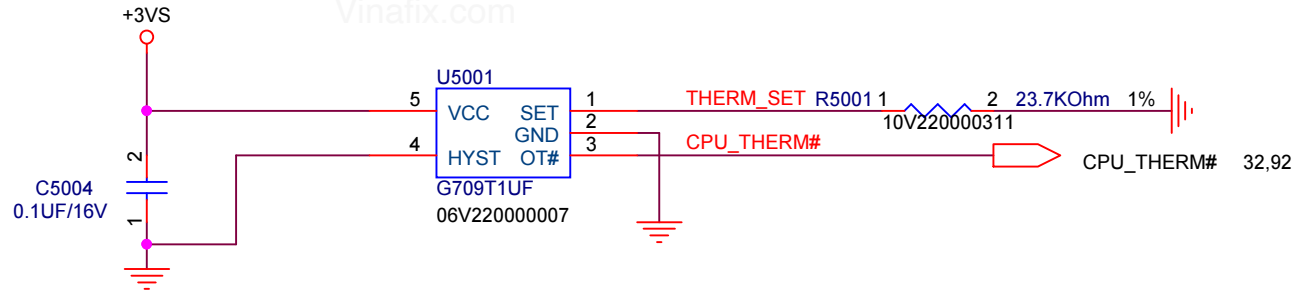
PEGATRON Title : **eMMC**

Engineer: **Raly Hsieh**

Size: **Custom** Project Name: **AS3EA** Rev: **2.0**

Date: **Monday, March 27, 2017** Sheet: **49** of **100**

+3VS +3VS 6,12,30,31,32,36,37,41,45,48,49,51,53,57,62,66,91,92
+5VS +5VS 31,36,48,57,69,91



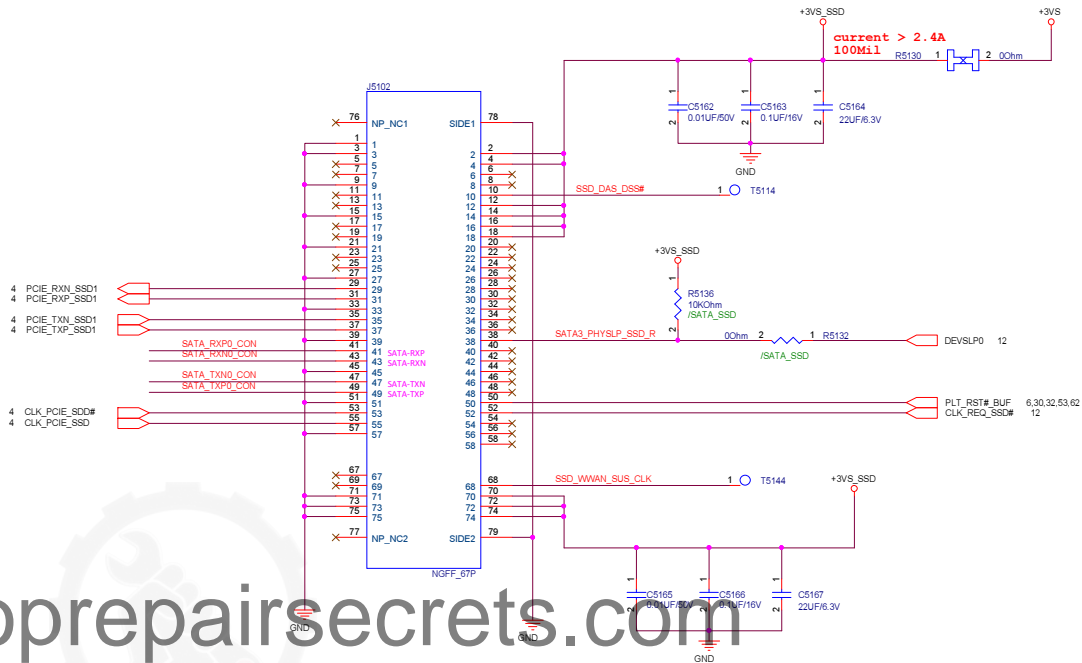
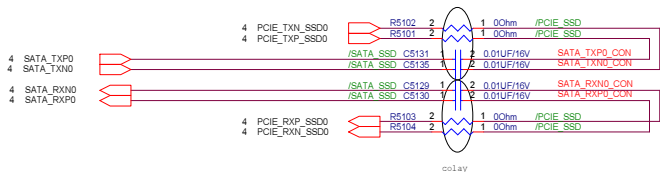
www.laptoprepairsecrets.com

PEGATRON		Title : THERMAL	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: Raly Hsieh	
Size	Project Name		Rev
Custom	AS3EA		2.0
Date:	Monday, March 27, 2017	Sheet	50 of 100

SATA SSD NGFF socket (M-key)

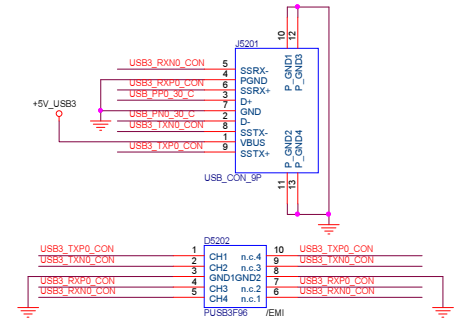
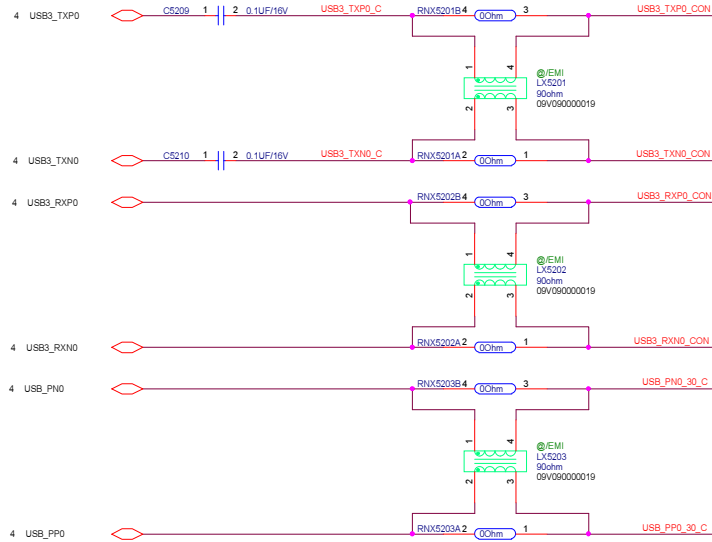
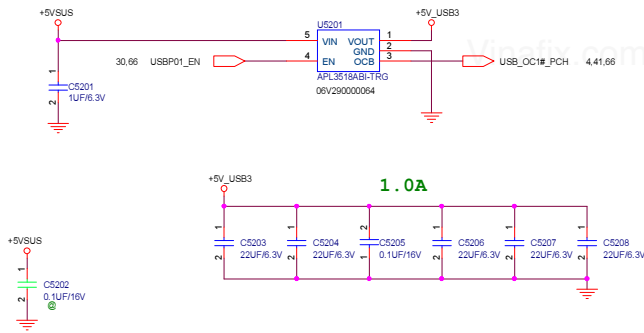
+3VS 6,12,30,31,32,36,37,41,45,48,49,50,53,57,62,66,91,92
+5VS 31,36,48,57,69,91

Vinafix.com

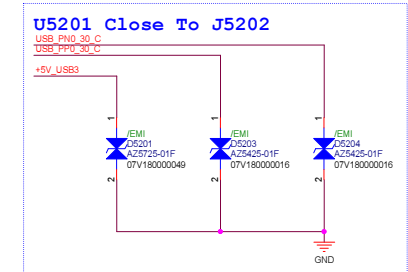


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52 USB3.0 Port 0



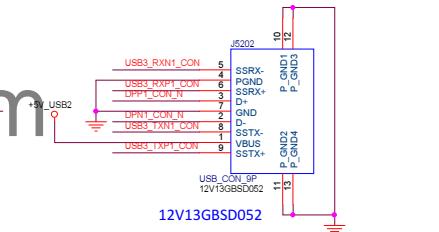
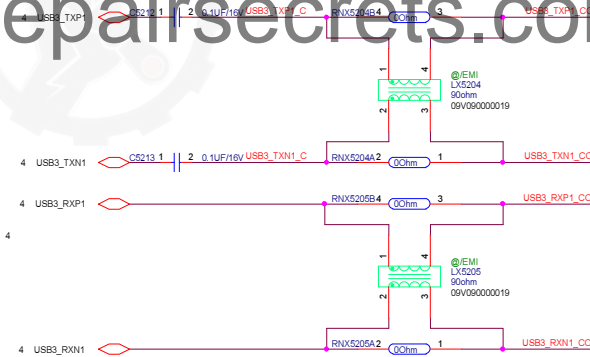
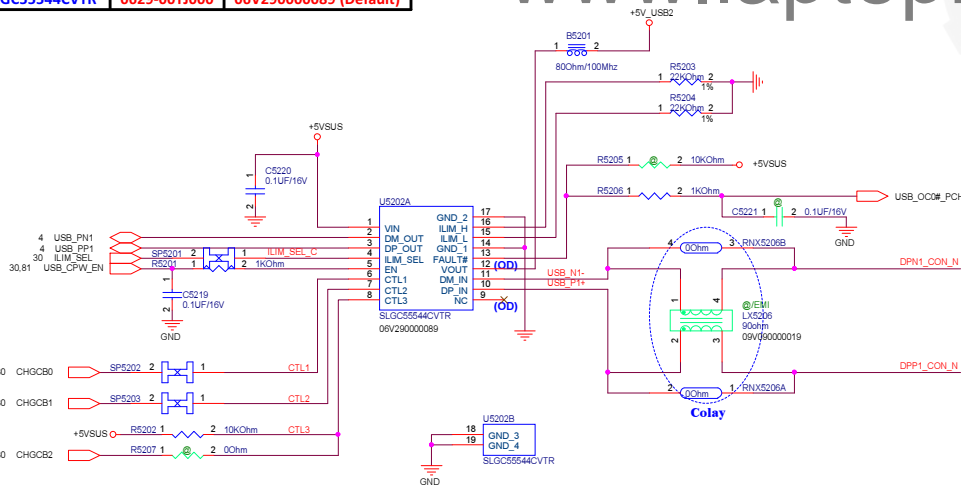
PLACE ESD Diodes near USB Connector



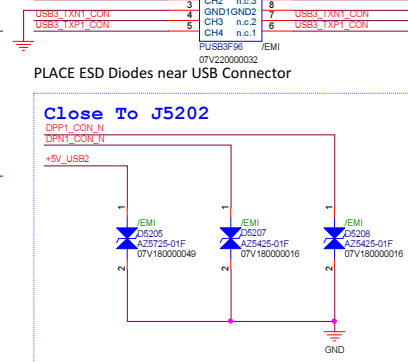
USB3.0 Port 1 S&C

Device	Pega No.	VX No.
SLGC55544CVTR	0629-00TJ000	06V290000089 (Default)

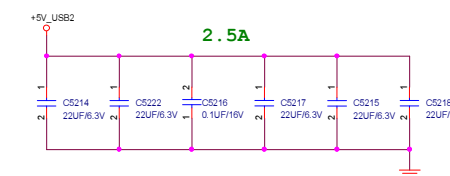
www.laptoprepairsecrets.com



PLACE ESD Diodes near USB Connector



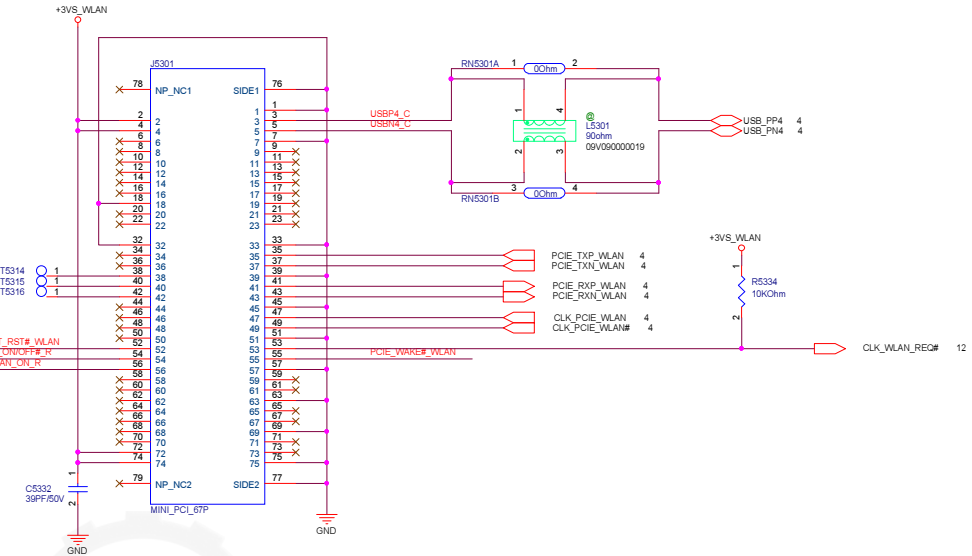
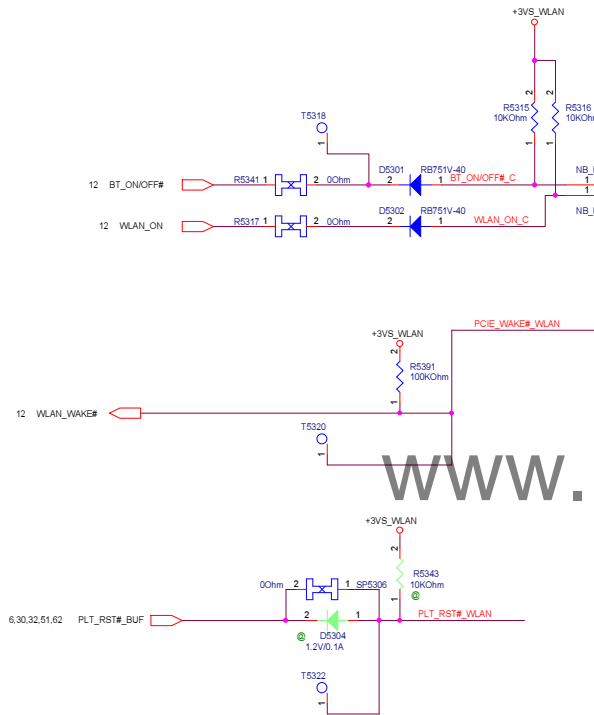
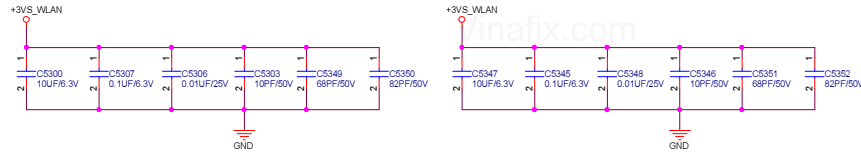
System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BCL2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO



+3V_WLAN_WP1 bypass capacitor:

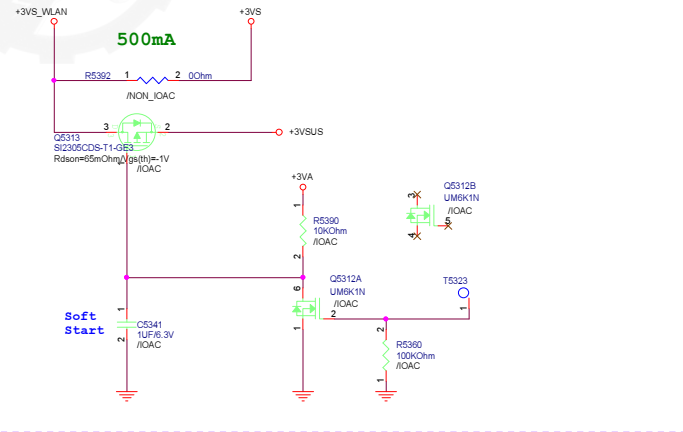
+3V_WLAN_WP1 bypass capacitor:

WLAN / BT



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IOAC Control Schematic



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PEGATRON		Title : <u>USB_HUB</u>	
<small>BG1-HW3 RD</small>		Engineer: <u>Raly Hsieh</u>	
<small>Size</small>	<small>Project Name</small>	<small>Rev</small>	
<u>Custom</u>	<u>AS3EA</u>	<u>2.0</u>	
<small>Date: <u>Monday, March 27, 2017</u></small>		<small>Sheet</small>	<small>54 of 100</small>

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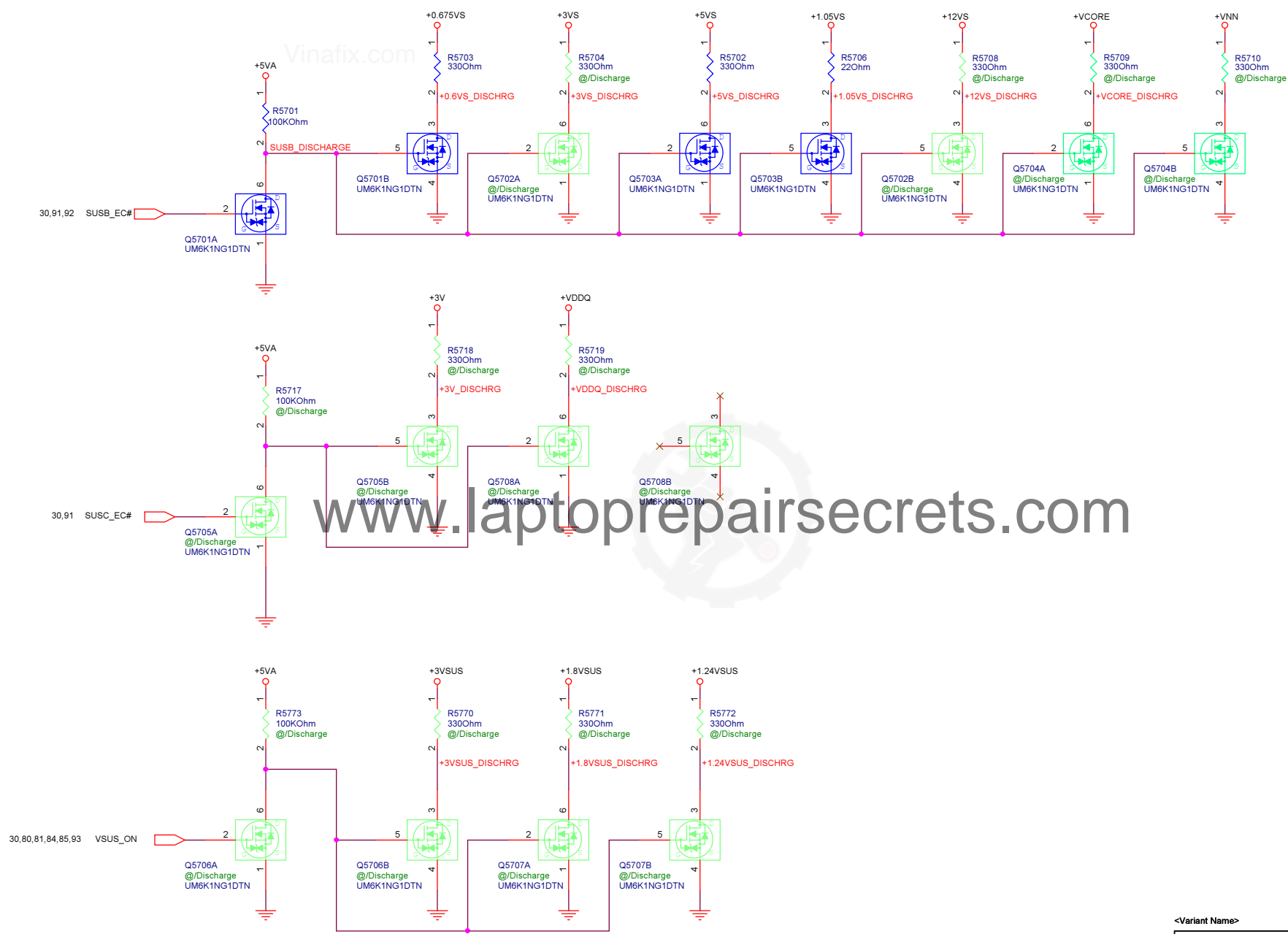
www.laptoprepairsecrets.com

PEGATRON		Title: SATA SSD_HDD	
<small>PEGATRON PROPRIETARY AND CONFIDENTIAL</small>			
<small>831-NS4</small>		Engineer: Raly Hsieh	
Size	Project Name		Rev
C	AS3EA		2.0
Date: Monday, March 27, 2017		Sheet	66 of 100

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PEGATRON		Title : LED	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Raly Hsieh	
Size	Project Name		Rev
Custom	AS3EA		2.0
Date: Monday, March 27, 2017		Sheet 56 of 100	



<Variant Name>		
PEGATRON Title : Discharge		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
Engineer: Raly Hsieh		
Size	Project Name	Rev
Custom	AS3EA	2.0
Date: Monday, March 27, 2017	Sheet 57	of 100

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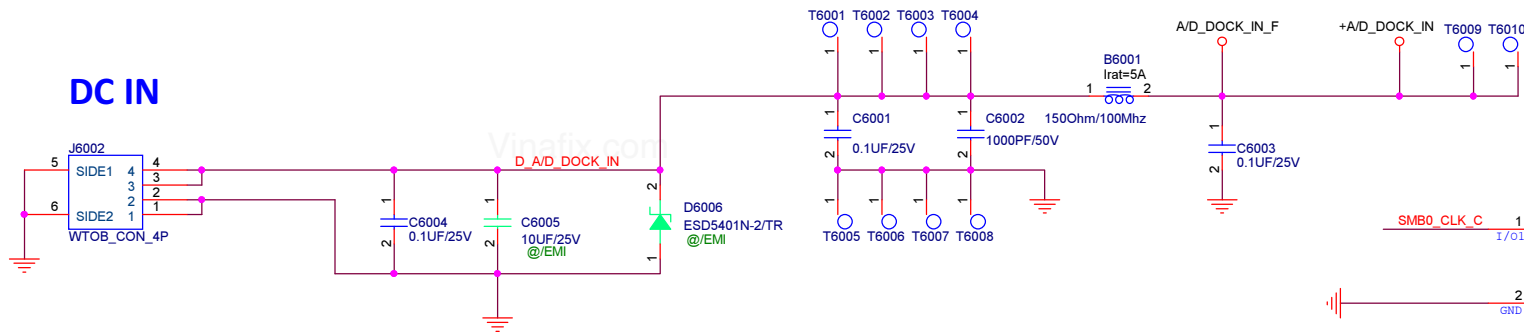
www.laptoprepairsecrets.com

PEGATRON		Title : ASM1042	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RD Center-HW RD Div.2-HW RD		Engineer: Raly Hsieh	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	56 of 100

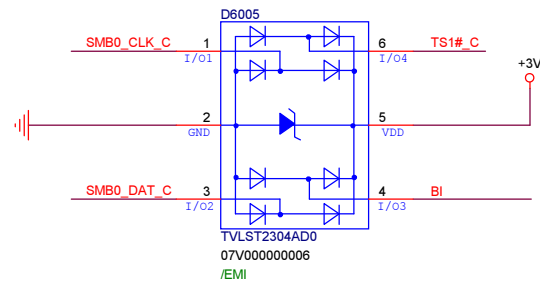
Vinafix.com

www.laptoprepairsecrets.com

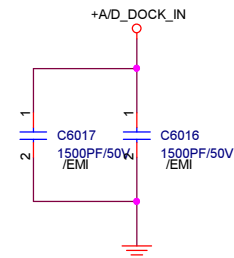
DC IN



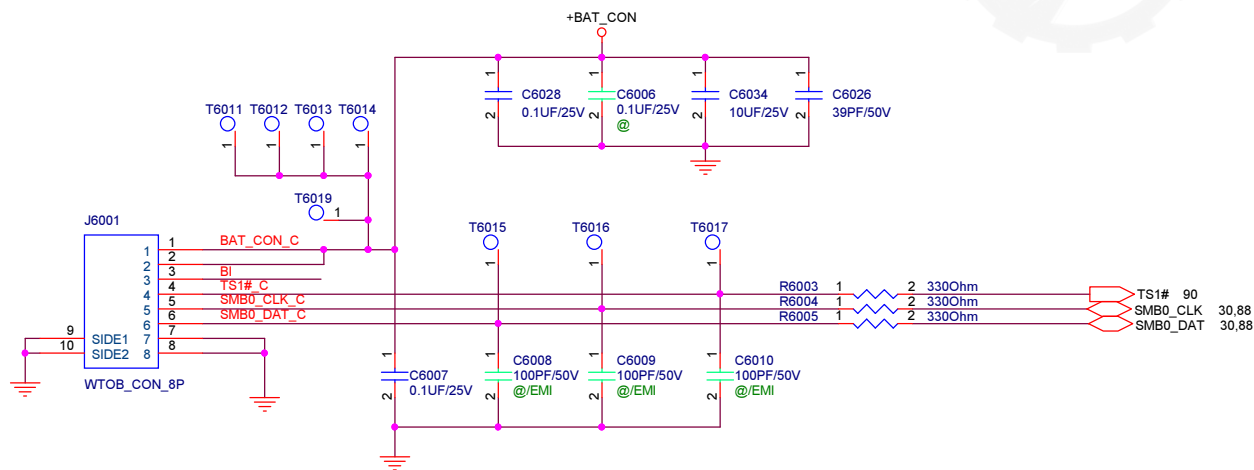
+BAT_CON 88
+3VA 9,30,31,36,53,65,81,88,93
+A/D_DOCK_IN 88



EMI



Battery Connector



PEGATRON Title : DC-IN/ Batt connector
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 Engineer: Raly Hsieh

Size Project Name AS3EA Rev 2.0

Date: Monday, March 27, 2017 Sheet 60 of 100

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<Variant Name>

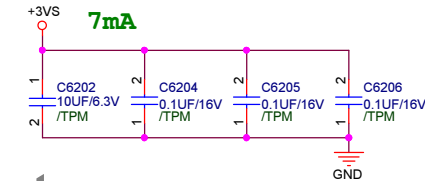
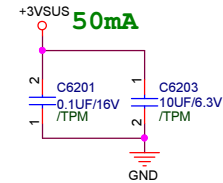
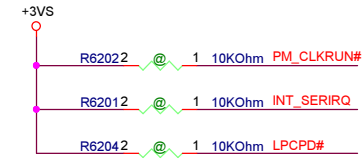
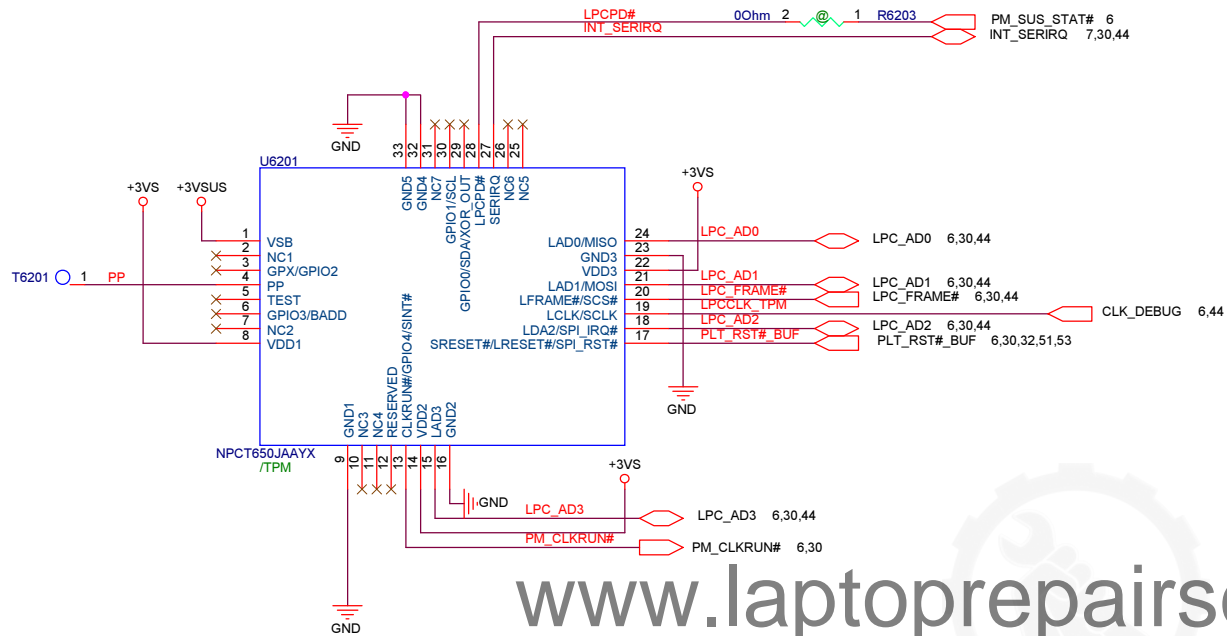
PEGATRON Title : Touch Panel Conn
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Raly Hsieh

Size Custom	Project Name	Rev 2.0
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Date: Monday, March 27, 2017 Sheet 61 of 100

Vinafix.com

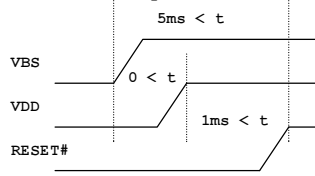


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TPM

VDD: Power the I/O buffers of the GPIO ports and the Host Interface
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.

TPM Power Sequence



NOTE: RESET# is LRESET#, SPI_RST# or SRESET#.

NOTE:

- 1) For TPM 1.2:
The TPM VSB pin must be connected to the system's standby voltage (existing at S3 power state).
- 2) For TPM 2.0:
It is recommended to connect the TPM VSB pin to the system's standby voltage to improve performance.
- 3) TPM VDD pins should be connected to the same power rail that feeds the Chipset LPC interface.
- 4) RESET# must be asserted for at least 5 msec after VSB power-up.
- 5) VSB may come up anytime before VDD power-up, but not after VDD power-up.
- 6) RESET# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.

PEGATRON Title : **TPM NPCT650**

BG1-NB4

Engineer: **Raly Hsieh**

Size	Project Name	Rev
B	AS3EA	2.0
Date: Monday, March 27, 2017	Sheet 62 of 100	

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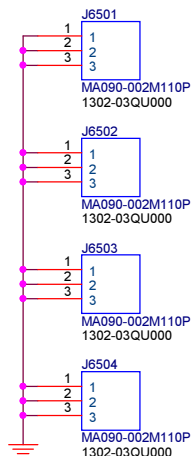
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	63 of 100

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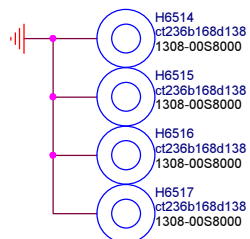
www.laptoprepairsecrets.com

PEGATRON		Title : IO Board	
931-R54		Engineer: Raly Hsieh	
Size C	Project Name AS3EA	Rev 2.0	
Date: Monday, March 27, 2017		Sheet	64 of 100

CLIP JCT



CPU NUTx4



WLAN NUT

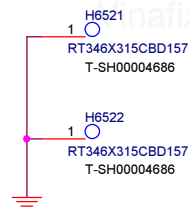


Thermal NUT

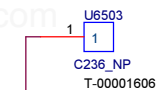


ME Screw Hole

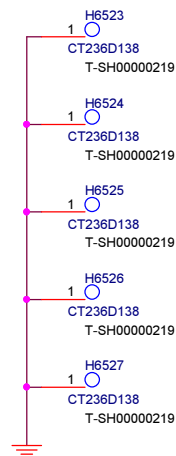
Screw Hole A



Screw Hole B



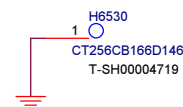
Screw Hole C



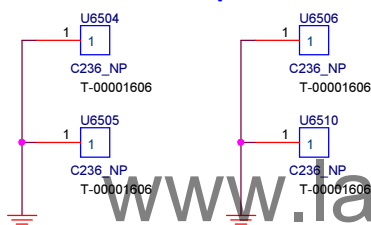
Screw Hole D



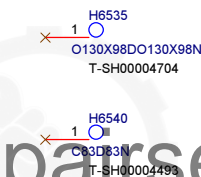
Screw Hole E



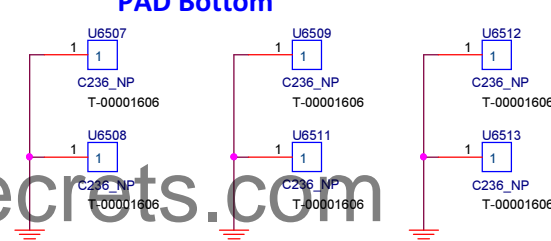
PAD Top



Tooling Hole

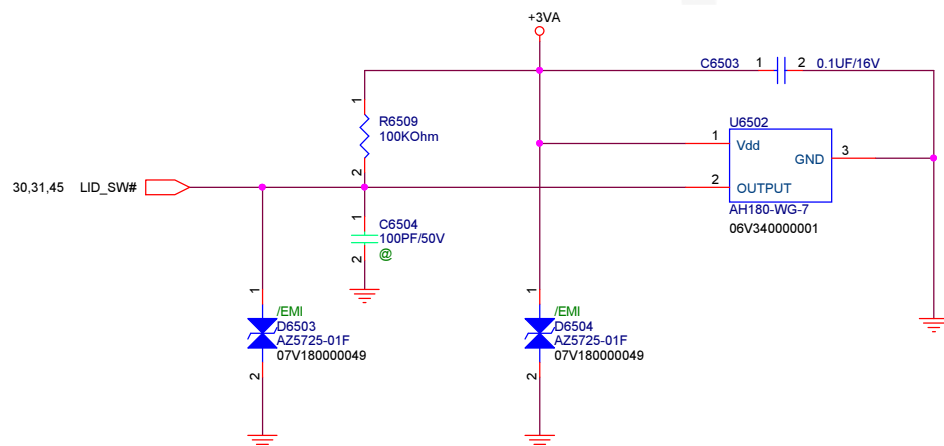


PAD Bottom



H6534	
1	P_GND
2	NP_NC2
3	NP_NC3
4	NP_NC4
5	NP_NC5
6	NP_NC6
7	NP_NC7
8	NP_NC8
9	NP_NC9
10	NP_NC10
11	NP_NC11
12	NP_NC12
13	NP_NC13
14	NP_NC14
15	NP_NC15
16	NP_NC16
17	NP_NC17
18	NP_NC18
19	NP_NC19
20	NP_NC20
21	NP_NC21
22	NP_NC22
23	NP_NC23
24	NP_NC24
25	NP_NC25
26	NP_NC26
27	NP_NC27
28	NP_NC28
29	NP_NC29
30	NP_NC30
31	NP_NC31
32	NP_NC32
33	NP_NC33
34	NP_NC34
35	NP_NC35
36	NP_NC36
37	NP_NC37
38	NP_NC38
39	NP_NC39
40	NP_NC40
41	NP_NC41
42	NP_NC42
43	NP_NC43
44	NP_NC44
45	NP_NC45
46	NP_NC46
47	NP_NC47
48	NP_NC48
49	NP_NC49
50	NP_NC50
51	NP_NC51
52	NP_NC52
53	NP_NC53
54	NP_NC54
55	NP_NC55
56	NP_NC56
57	NP_NC57
58	NP_NC58
59	NP_NC59
60	NP_NC60
61	NP_NC61

Hall Sensor



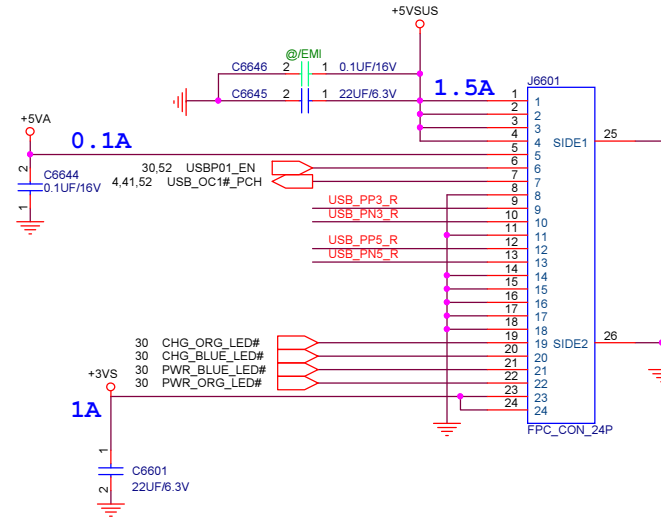
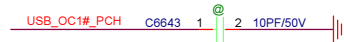
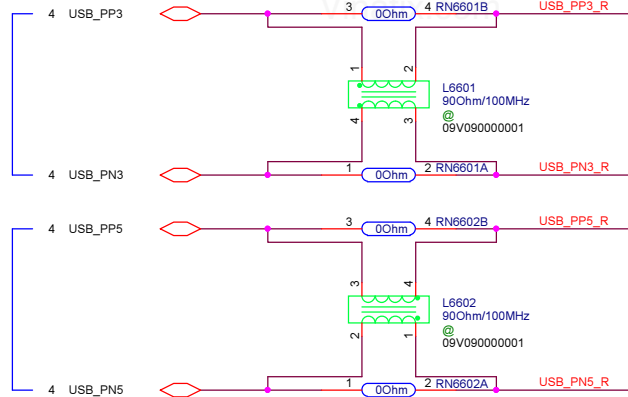
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PEGATRON		Title : ME_CONN,Skew Hole	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW3		Engineer: Raly Hsieh	
Size	Project Name		Rev
B	AS3EA		2.0
Date: Monday, March 27, 2017		Sheet	65 of 100

DB CONN

USB2.0 (IO)

CR



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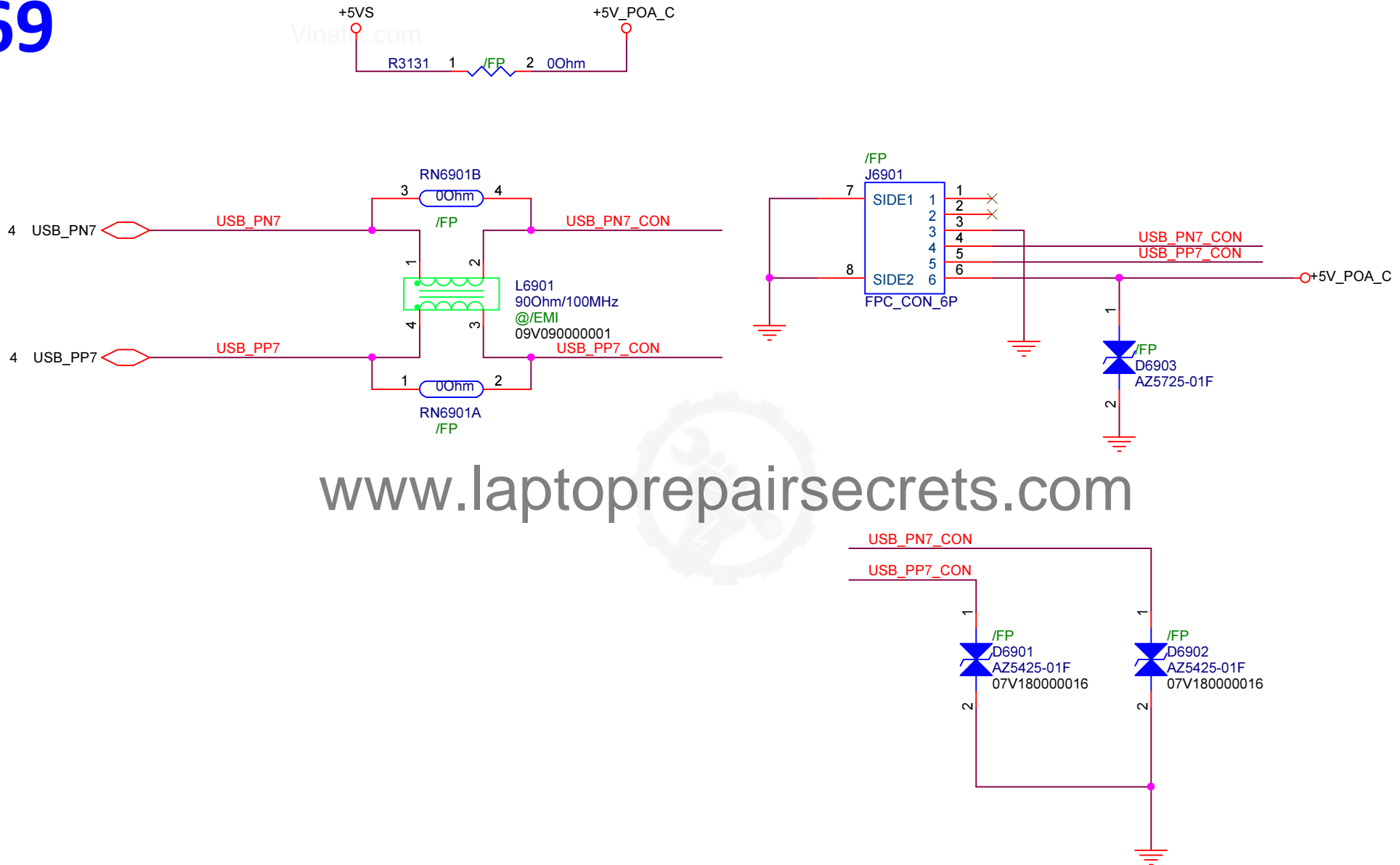
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<Variant Name>			
PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name AS3EA	Rev 2.0	
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PEGATRON Title : Finger printer		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1-NB4		
Engineer: Raly Hsieh		
Size A	Project Name AS3EA	Rev 2.0
Date: Monday, March 27, 2017		
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PEGATRON		Title : 70. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
Date: Monday, March 27, 2017		Sheet 70 of 100	

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PEGATRON		Title : 71. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
Date: Monday, March 27, 2017		Sheet 71 of 100	

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PEGATRON		Title : 72. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
Date: Monday, March 27, 2017		Sheet 72 of 100	

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PEGATRON		Title : 73. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
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PEGATRON		Title : 74. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
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PEGATRON		Title : 75. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
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PEGATRON		Title : 76. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
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PEGATRON		Title : 77. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
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PEGATRON		Title : 78. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
Date: Monday, March 27, 2017		Sheet 78 of 100	

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PEGATRON		Title : 79. *****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW4		Engineer: Raly Hsieh	
Size A	Project Name AS3EA		Rev 2.0
Date: Monday, March 27, 2017		Sheet 79 of 100	

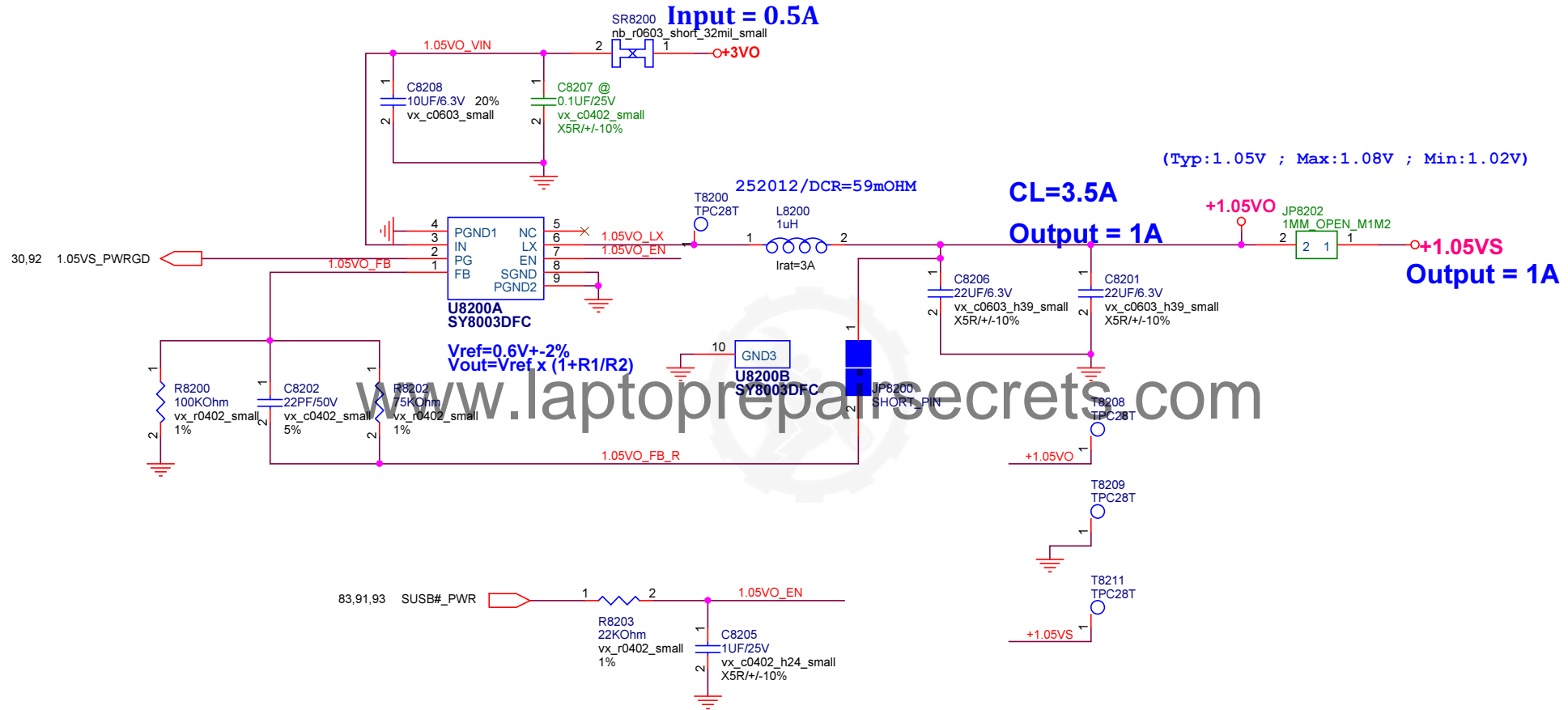


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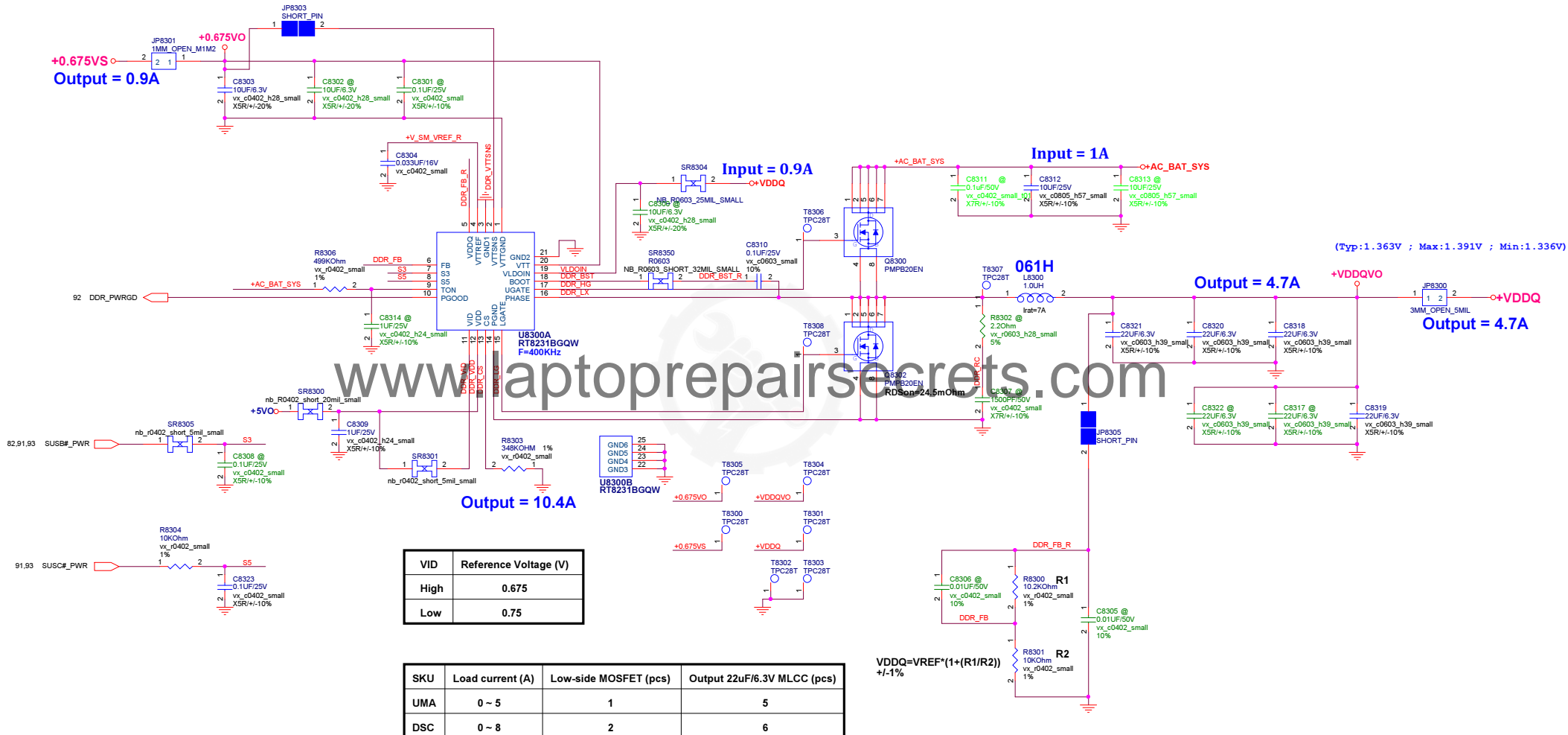


<Variant Name

+1.05VO POWER SUPPLY



DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

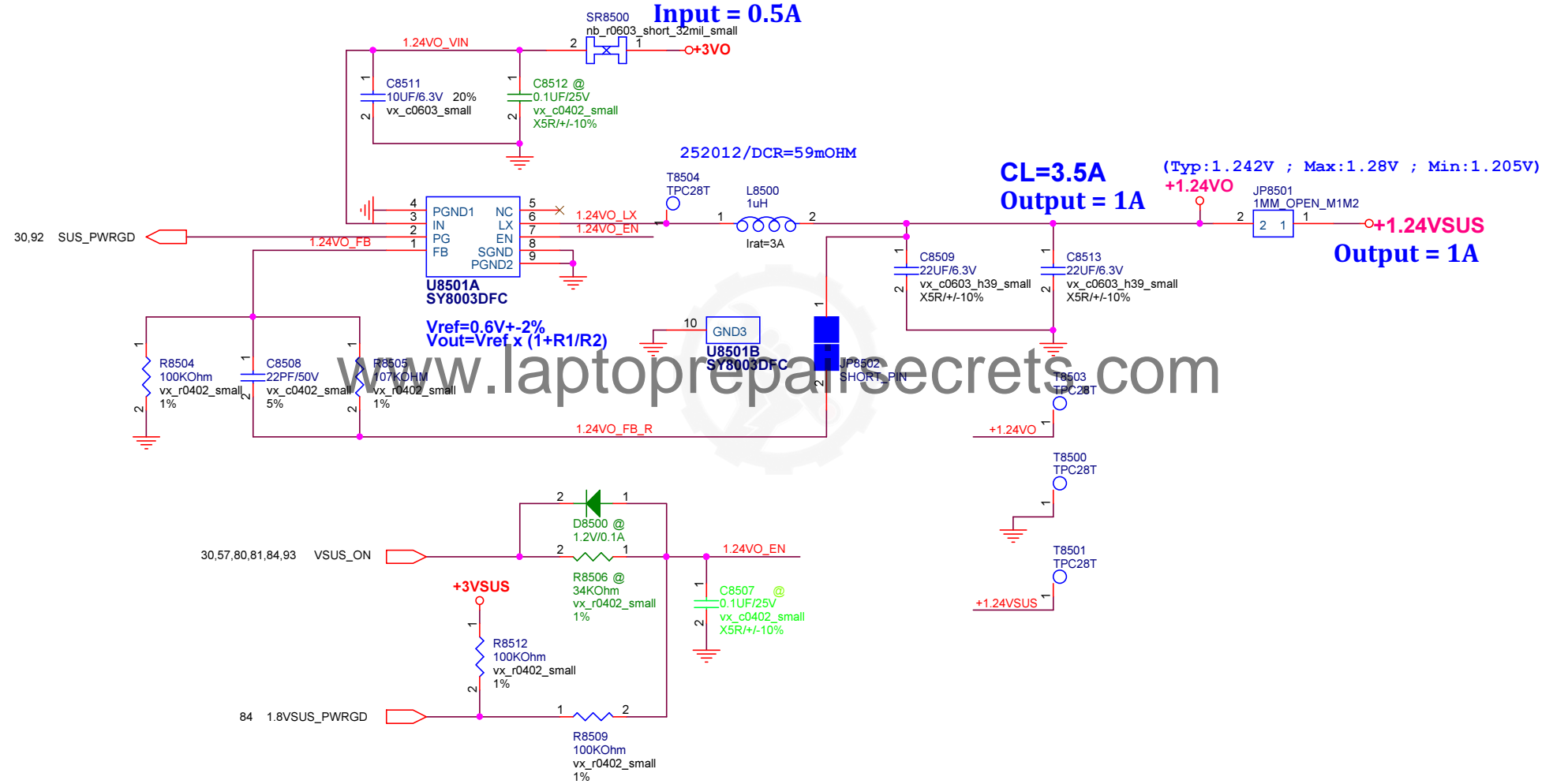
SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	5
DSC	0 ~ 8	2	6



PEGATRON		Title :	1.8VSUS
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer:	Neil Lin
Size Custom	Project Name	TJ13A	Rev 2.0
Date:	Monday, March 27, 2017	Sheet	84 of 100

+1.24VO POWER SUPPLY

Input = 0.5A



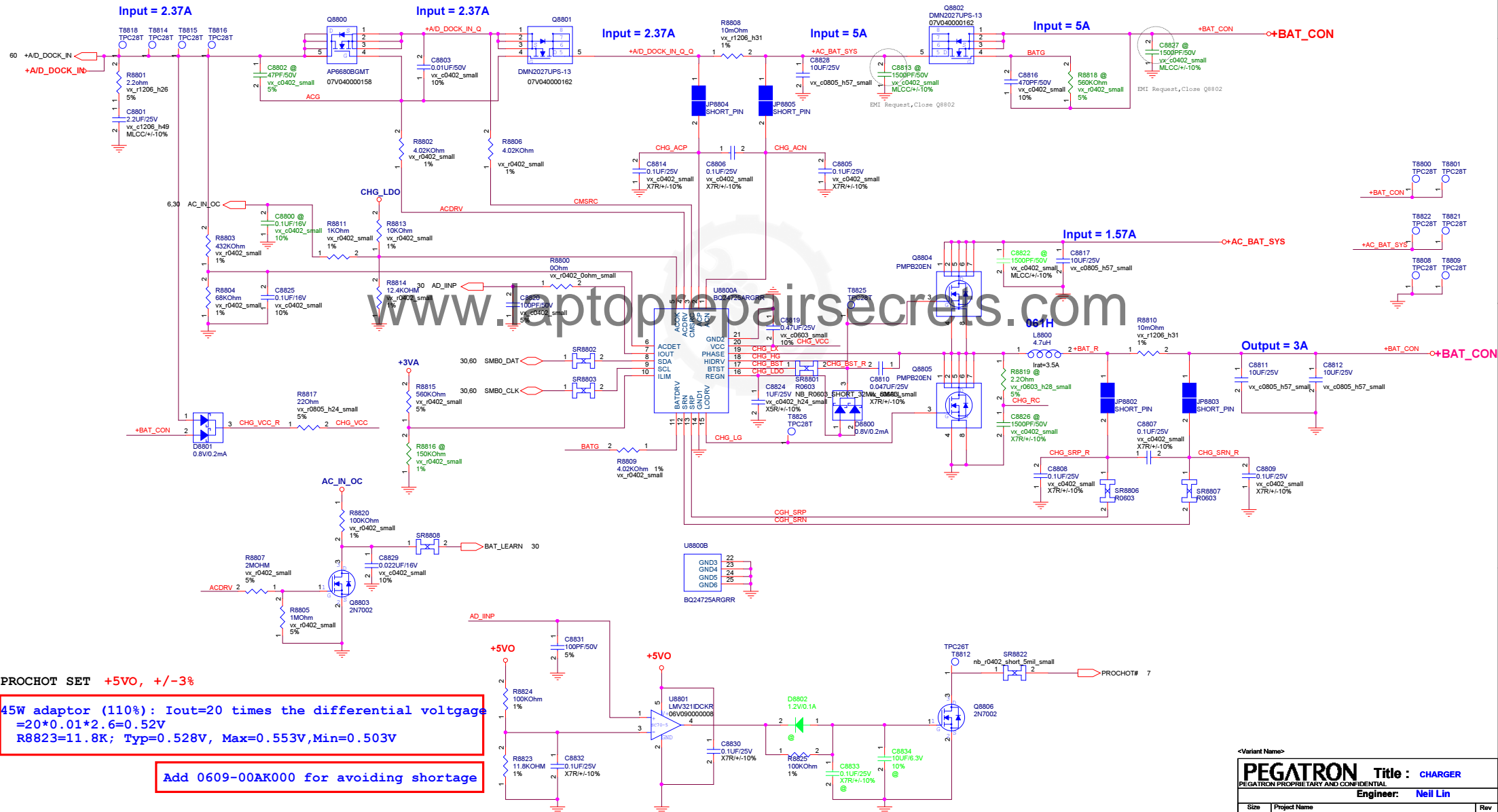
<Variant Name>

PEGATRON Title : 1.24VSUS
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Neil Lin

Size Custom	Project Name AS3EA	Rev 2.0
Date: Monday, March 27, 2017	Sheet 85 of 100	

BATTERY CHARGER



<Variant Name>

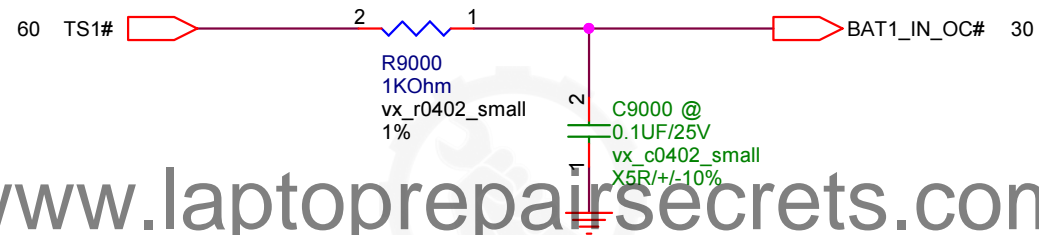
PEGATRON Title : CHARGER
 PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Neil Lin

Size	Project Name	Rev
Custom	AS3EA	2.0
Date:	Monday, March 27, 2017	Sheet 88 of 100

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BATTERY IN DETECT



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<Variant Name>

PEGATRON Title : **DETECT**
PEGATRON PROPRIETARY AND CONFIDENTIAL

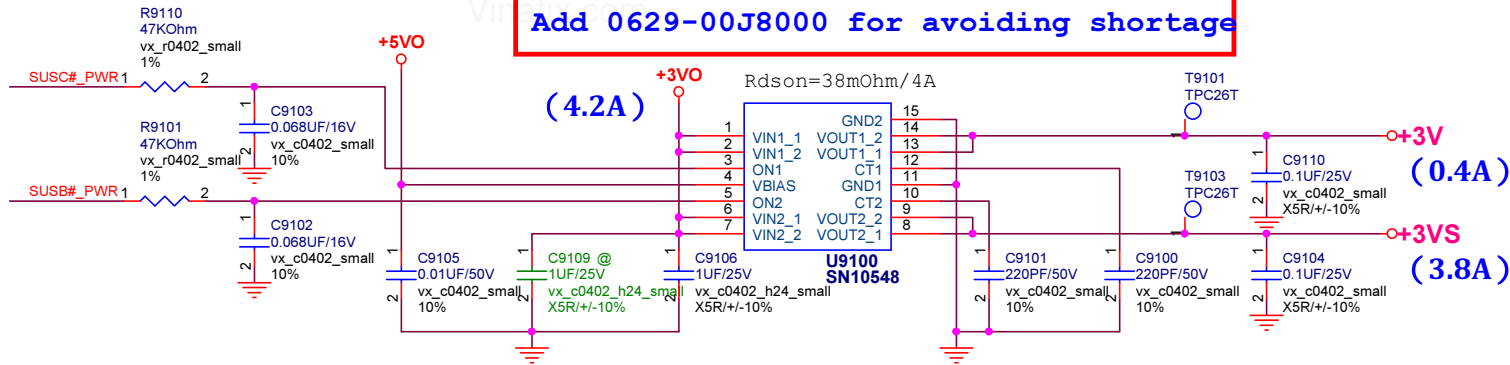
Engineer: **Neil Lin**

Size Custom	Project Name AS3EA	Rev 2.0
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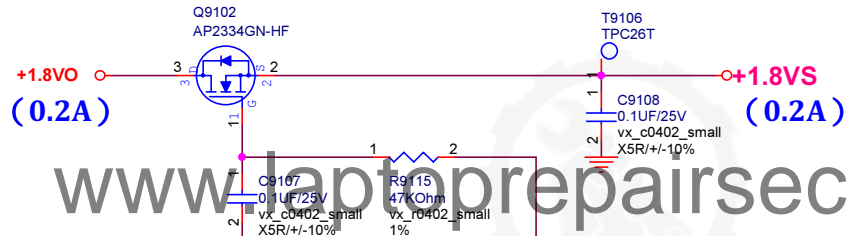
Date: **Monday, March 27, 2017** Sheet **90** of **100**

SUSB# & SUSC# POWER

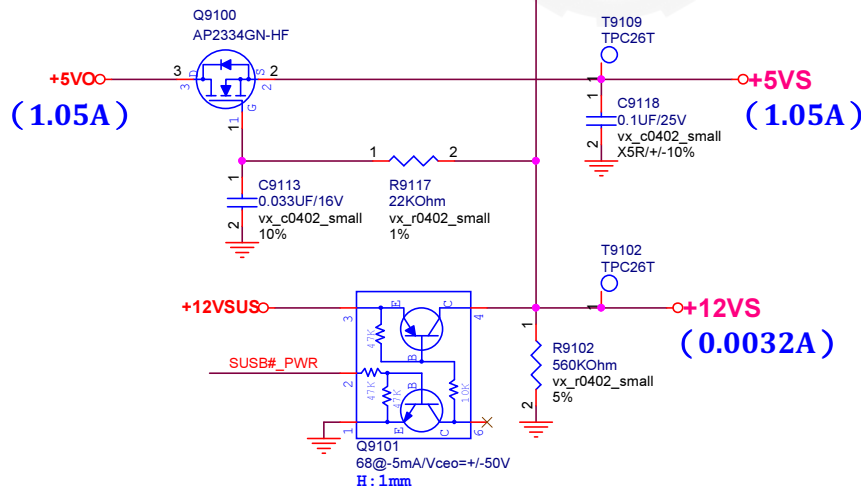
Add 0629-00J8000 for avoiding shortage



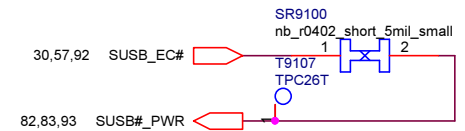
VGS=10V, RDson=27.6mOHM



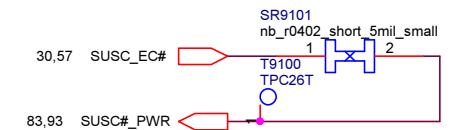
VGS=10V, RDson=27.6mOHM



SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



<Variant Name>

PEGATRON Title: SWITCH	
PEGATRON PROPRIETARY AND CONFIDENTIAL	
Engineer: Neil Lin	
Size Custom	Project Name AS3EA
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+A/D_DOCK_IN → +A/D_DOCK_IN 60,88
+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,83,88
+BAT_CON → +BAT_CON 60,88

+5VA → +5VA 57,66,81
+3VA → +3VA 9,30,31,36,53,60,65,81,88

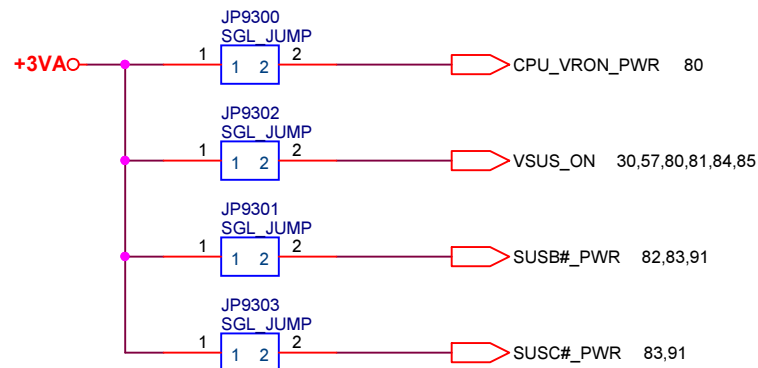
+5VO → +5VO 80,81,83,84,88,91
+3VO → +3VO 81,82,85,91
+1.8VO → +1.8VO 84,91
+1.24VO → +1.24VO 85
+VDDQVO → +VDDQVO 83
+1.05VO → +1.05VO 82
+0.675VO → +0.675VO 83

+12VSUS → +12VSUS 6,81,91
+3VSUS → +3VSUS 4,6,7,9,12,15,30,31,45,53,57,62,80,81,84,85,92
+5VSUS → +5VSUS 41,52,66,81
+1.8VSUS → +1.8VSUS 4,5,6,7,8,9,12,13,15,44,57,84
+1.24VSUS → +1.24VSUS 9,57,85

+VDDQ → +VDDQ 9,16,17,18,57,83
+12VS → +12VS 31,49,57,91
+5VS → +5VS 31,36,48,57,69,91
+3VS → +3VS 6,12,30,31,32,36,37,41,45,48,49,50,51,53,57,62,66,91,92
+1.8VS → +1.8VS 4,5,6,12,31,32,36,48,49,91
+1.05VS → +1.05VS 4,9,57,82
+0.675VS → +0.675VS 16,17,57,83

+VNN → +VNN 9,57,80
+VCORE → +VCORE 9,57,80
+3VA_EC → +3VA_EC 15,30,32,80

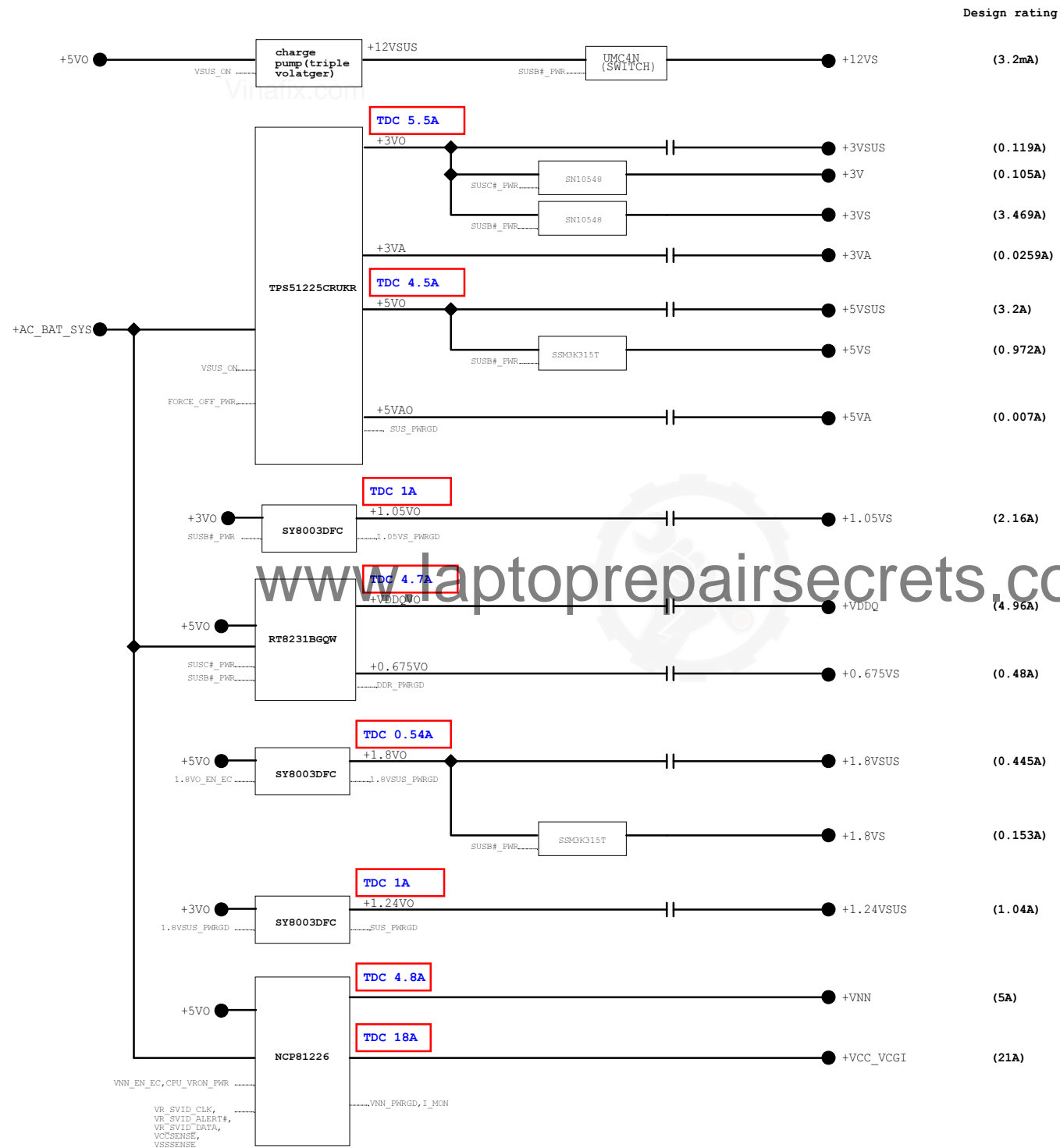
FOR POWER TEST



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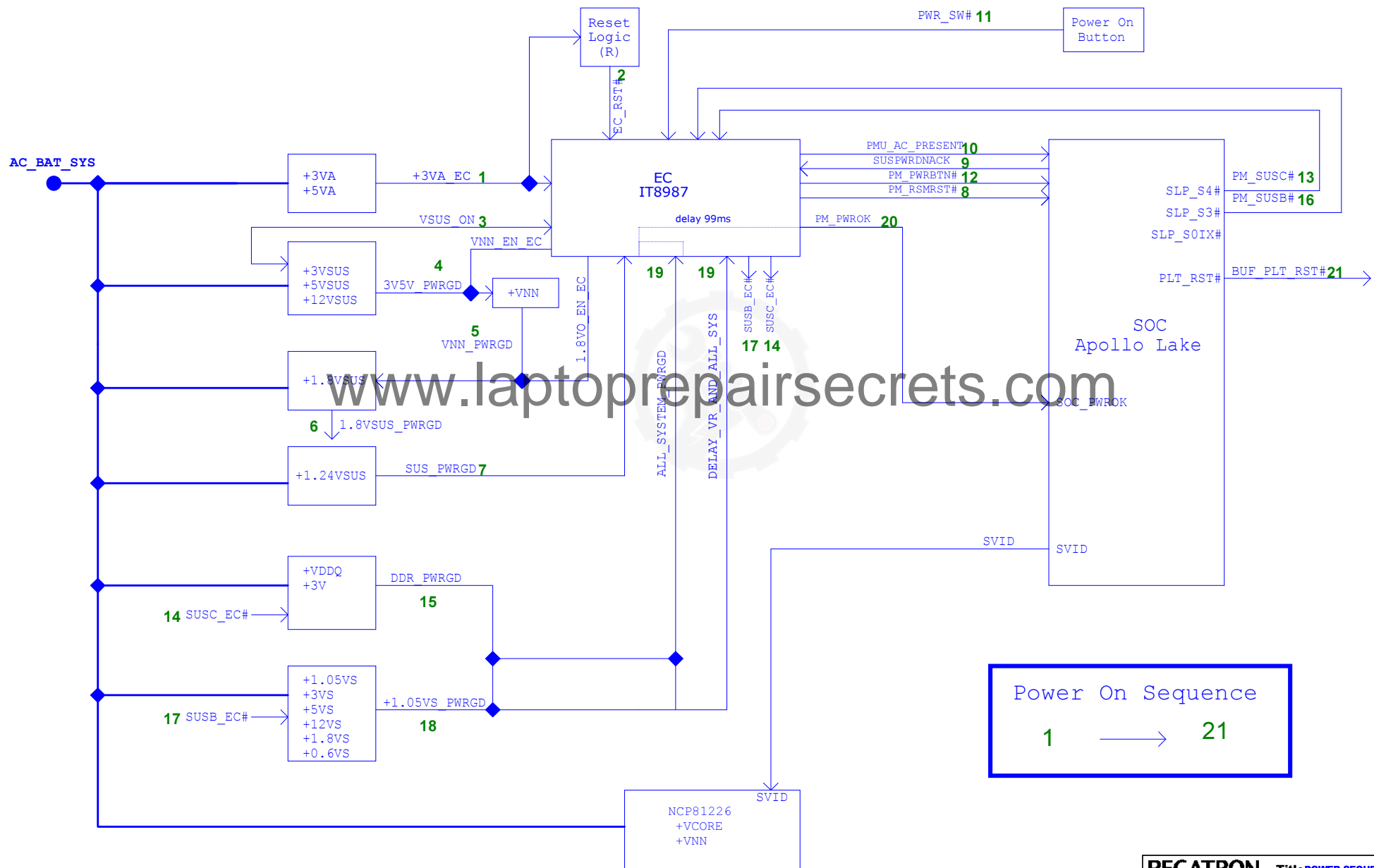
<Variant Name>

PEGATRON		Title : SIGNAL	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Size A4		Project Name AS3EA	
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Power On Sequence Diagram G3-S0 R0.1

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Power On Sequence

1 → 21

LED POWER LED

Charger LED

USB 2.0

